

648FX-M7 661FX-M7


Rev: A


Revision History :

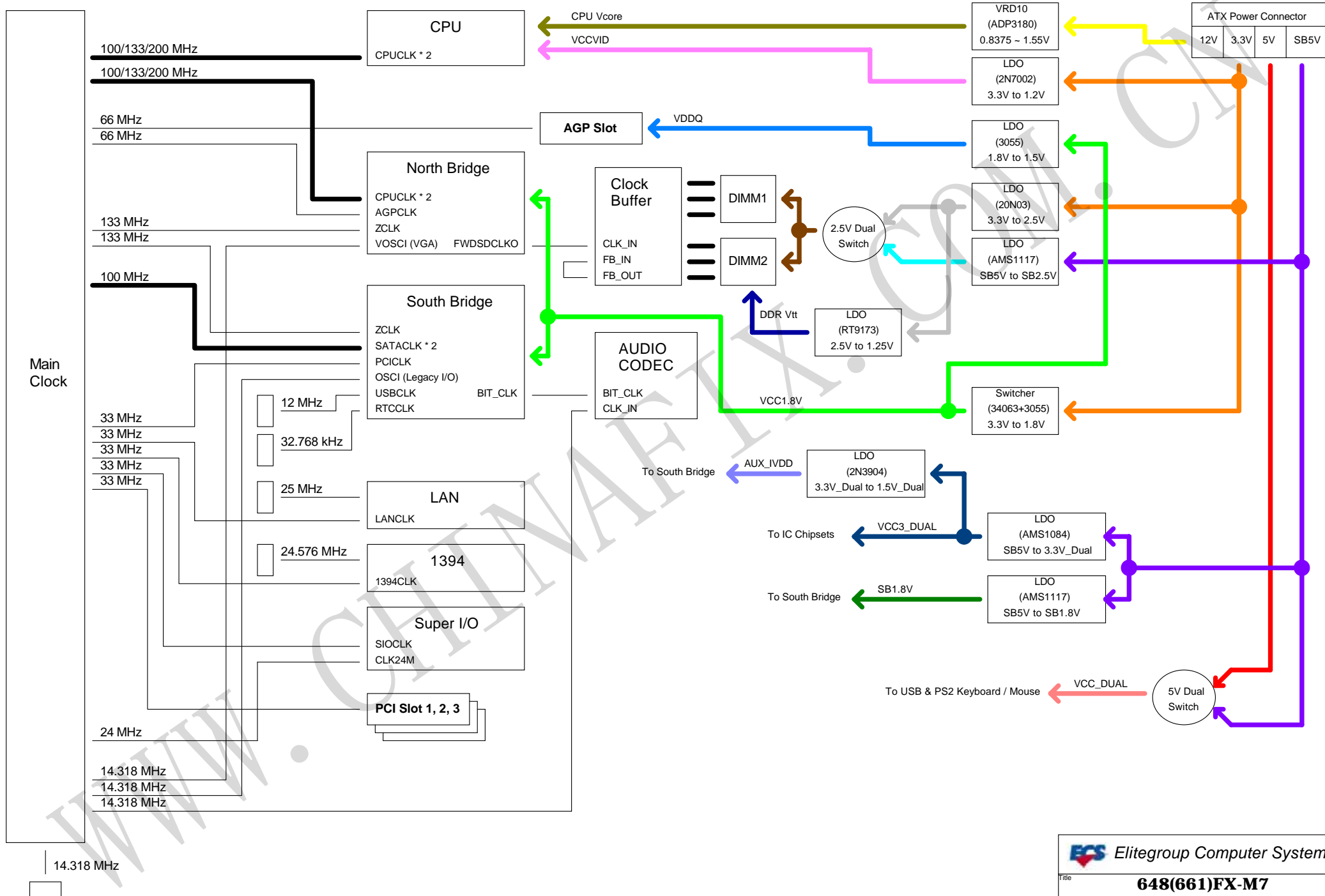
1. Ver A: Initial for 661FX/648FX for LGA775

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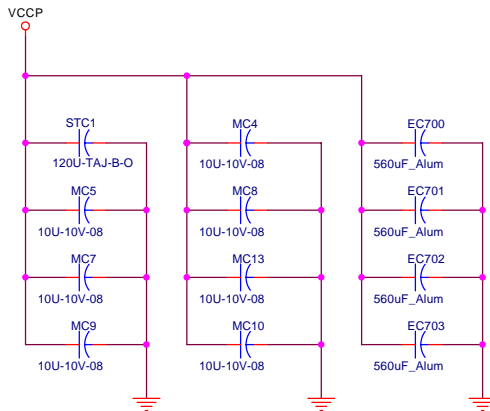
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	SIGNATURE	DATE
DESIGNER	LukeLin	
LAYOUT	ECS Layout team	
CHECK	LukeLin	
APPROVAL		

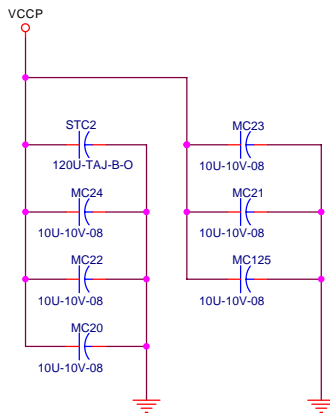
 Elitegroup Computer Systems		
Title 648(661)FX-M7		
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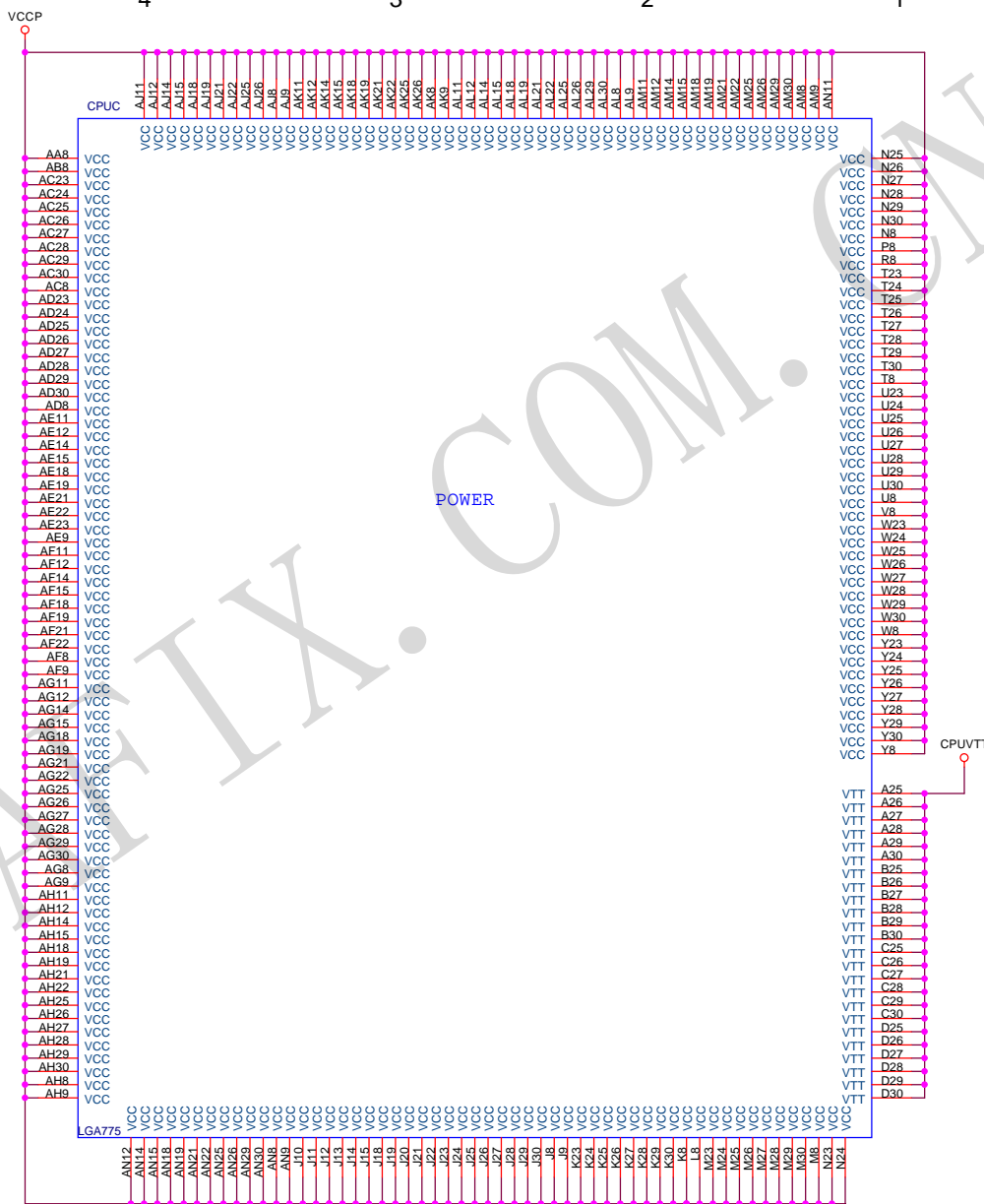
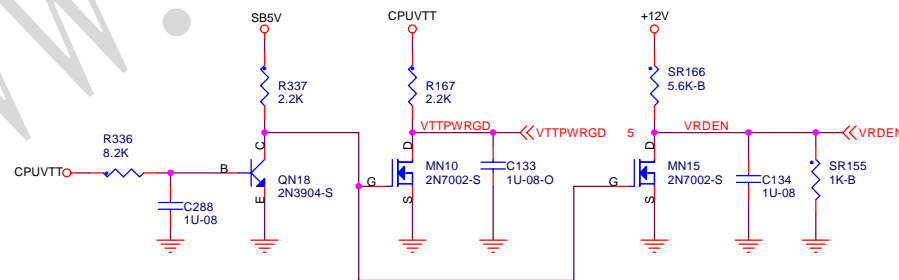
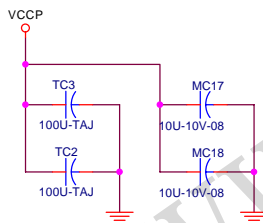
Put these capacitors at processor TOP SIDE

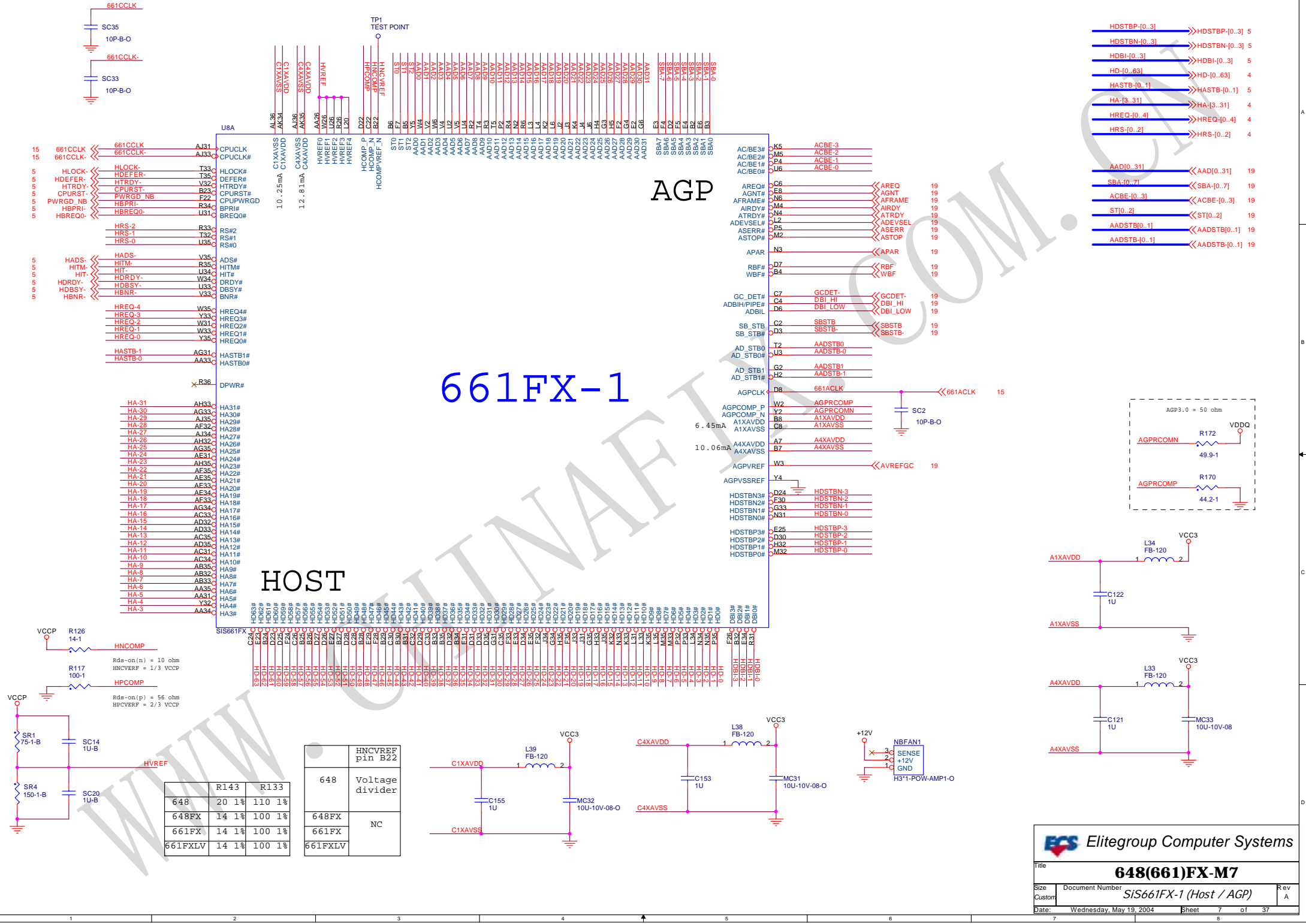


Put these capacitors at processor LEFT SIDE



Put these capacitors INSIDE PROCESSOR CAVITY





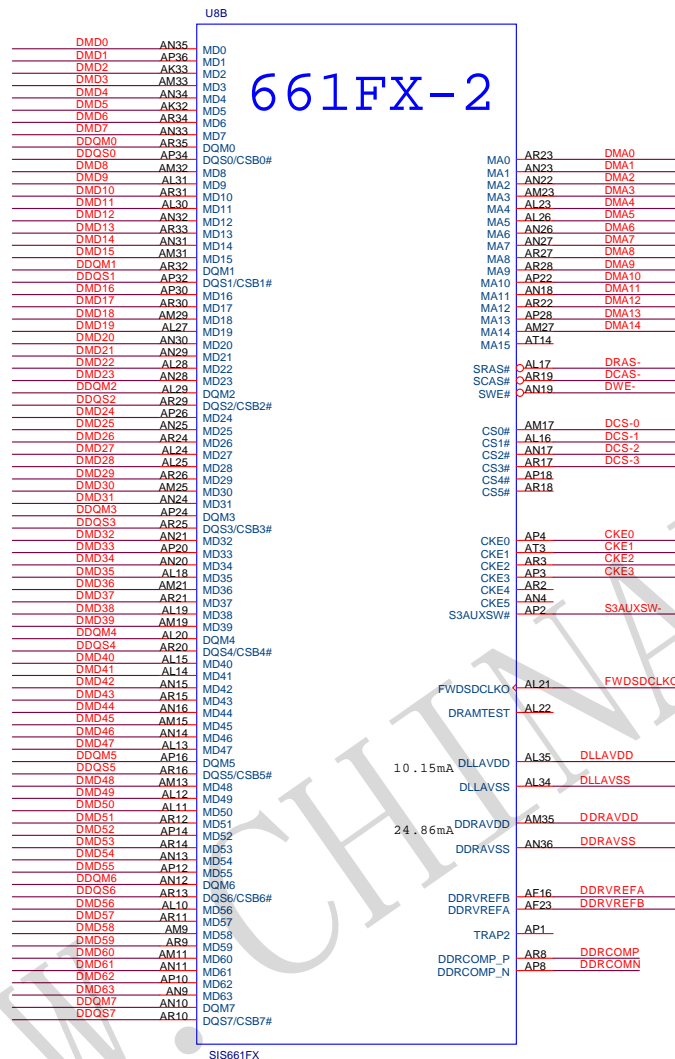
661FX-1

HOST

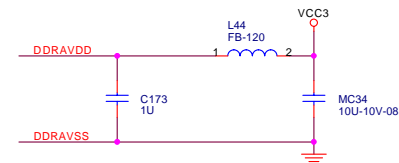
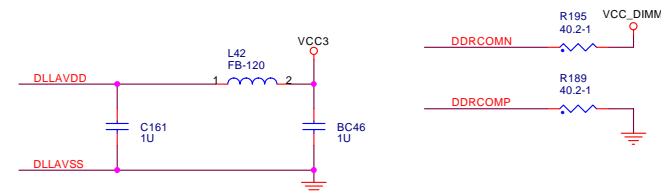
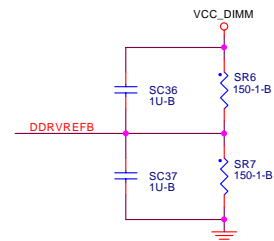
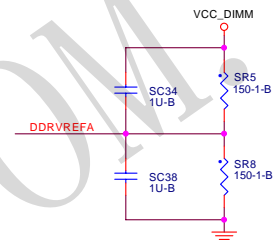
AGP

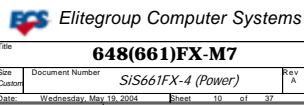
	R143	R133
648	20 1%	110 1%
648FX	14 1%	100 1%
661FX	14 1%	100 1%
661FXLV	14 1%	100 1%

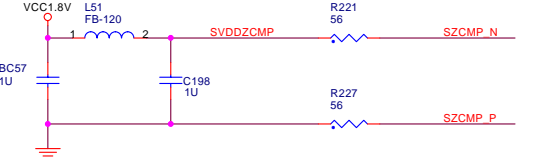
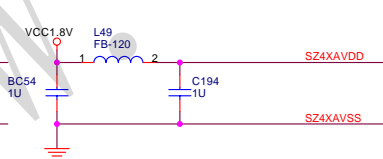
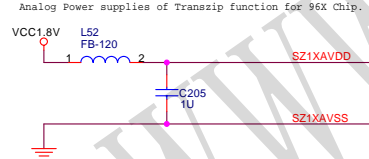
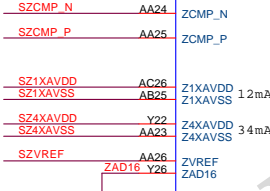
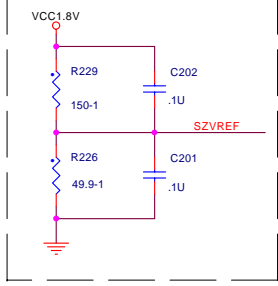
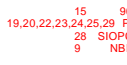
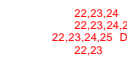
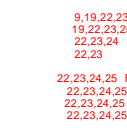
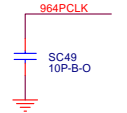
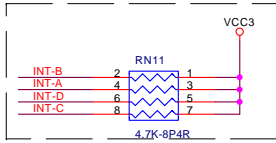
	HNCVREF pin B22
648	Voltage divider
648FX	NC
661FX	NC
661FXLV	NC



DMD[0..63]	<< DMD[0..63]	17,18
DDQM[0..7]	<< DDQM[0..7]	17,18
DDQS[0..7]	<< DDQS[0..7]	17,18
DMA[0..14]	<< DMA[0..14]	17,18
DCS[0..3]	<< DCS[0..3]	17,18
CKE[0..3]	<< CKE[0..3]	17





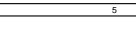
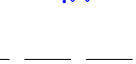
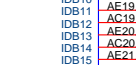
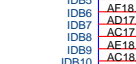
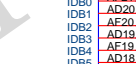
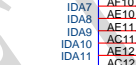
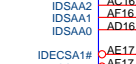
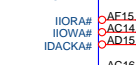


PCI

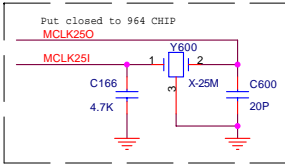
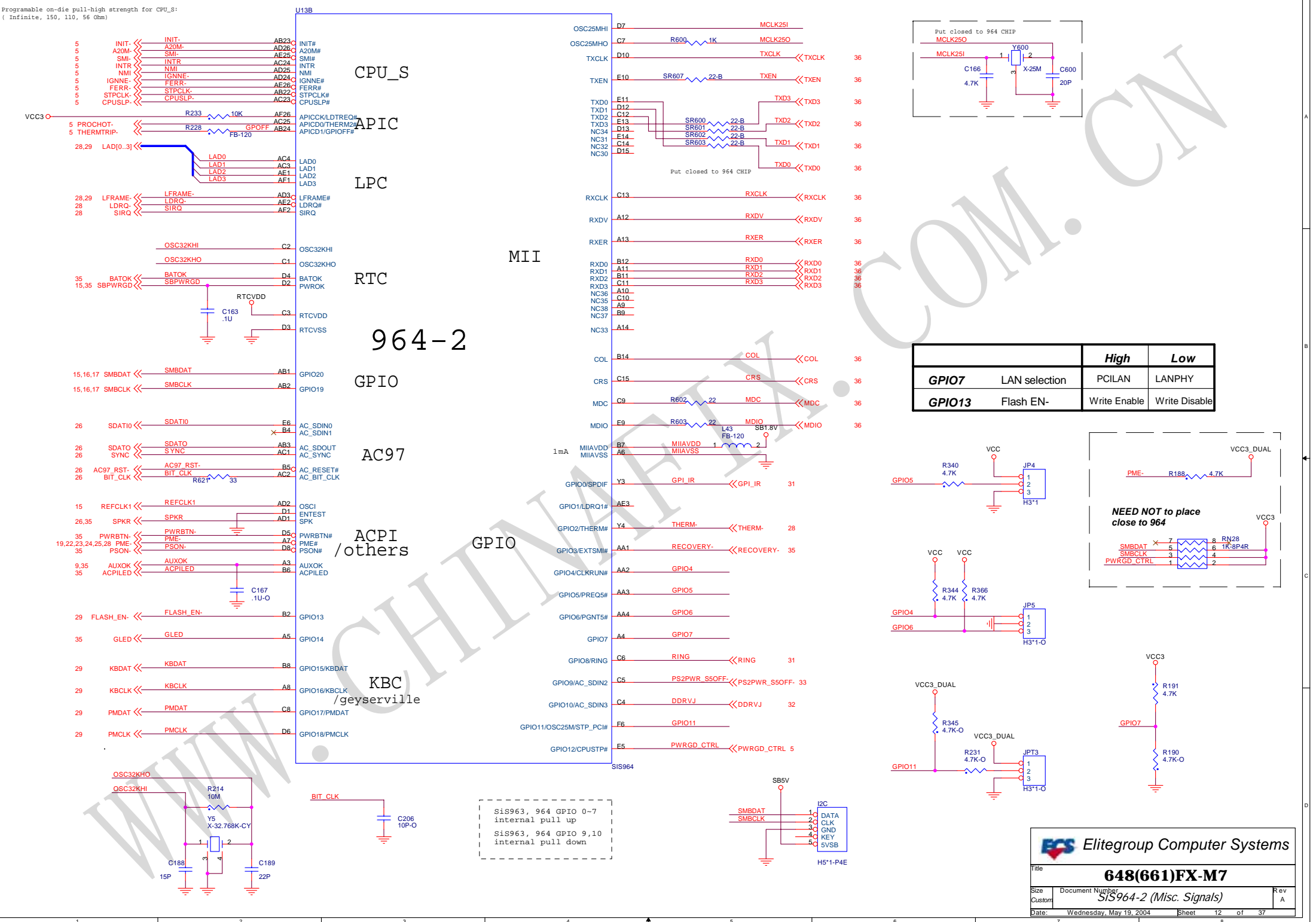
IDE

964-1

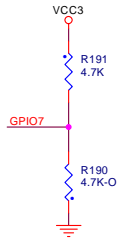
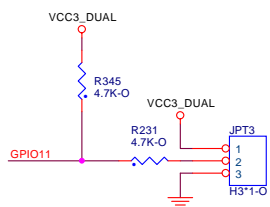
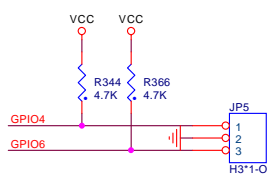
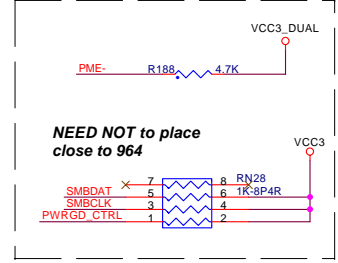
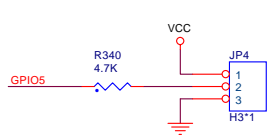
HyperZip



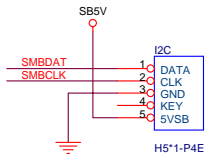
Programmable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)

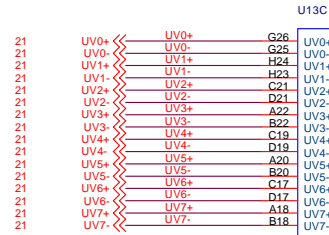
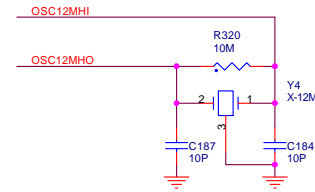
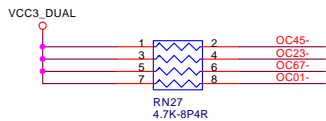


		High	Low
GPIO7	LAN selection	PCILAN	LANPHY
GPIO13	Flash EN-	Write Enable	Write Disable



SIS963, 964 GPIO 0-7
internal pull up
SIS963, 964 GPIO 9,10
internal pull down

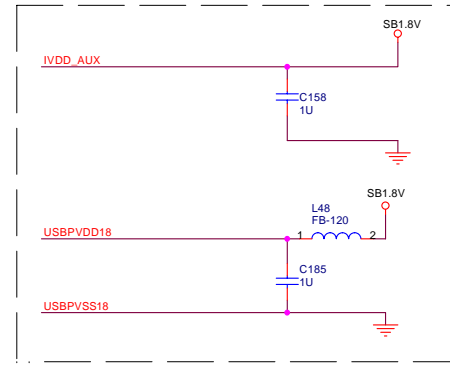
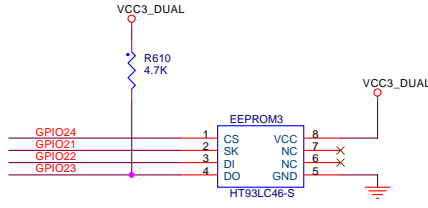
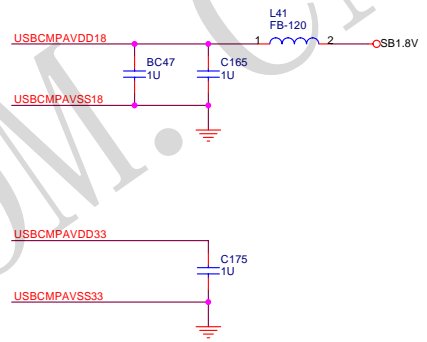
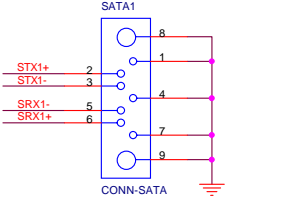
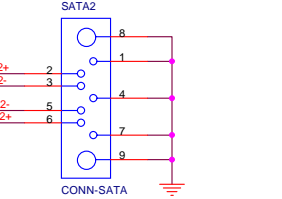
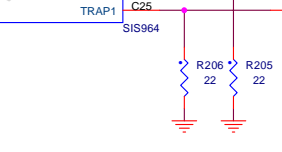
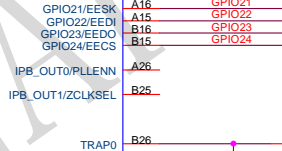
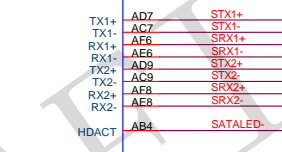
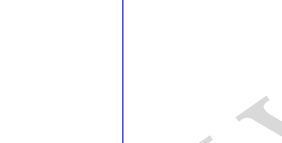
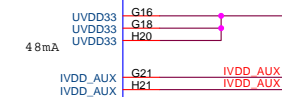
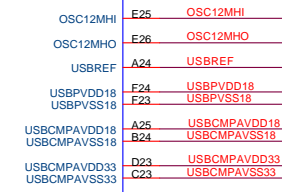
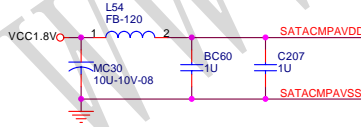
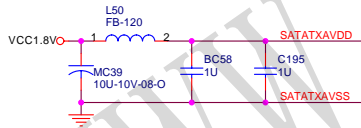
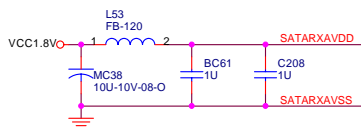
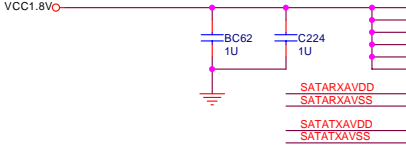
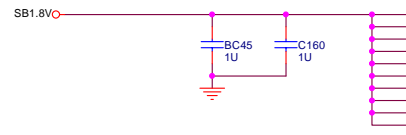


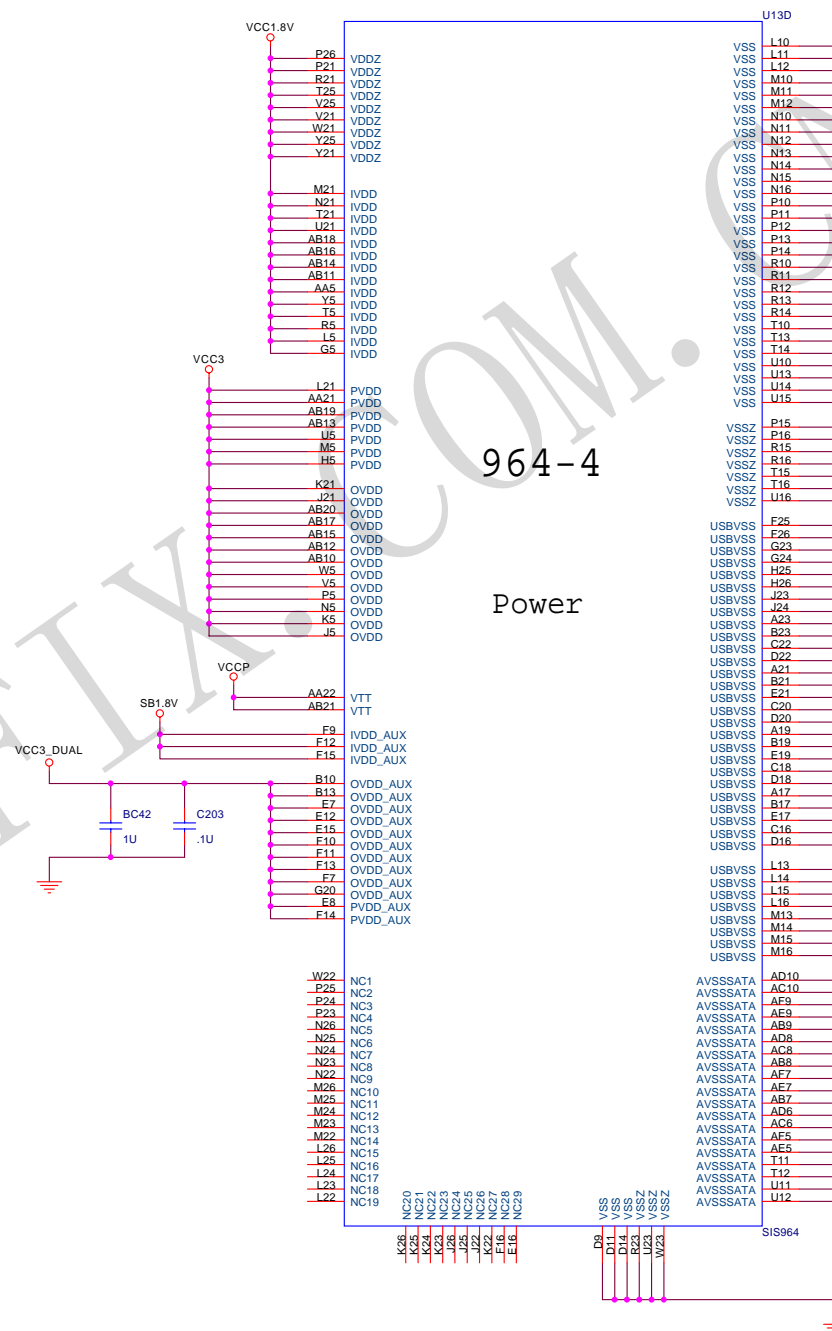
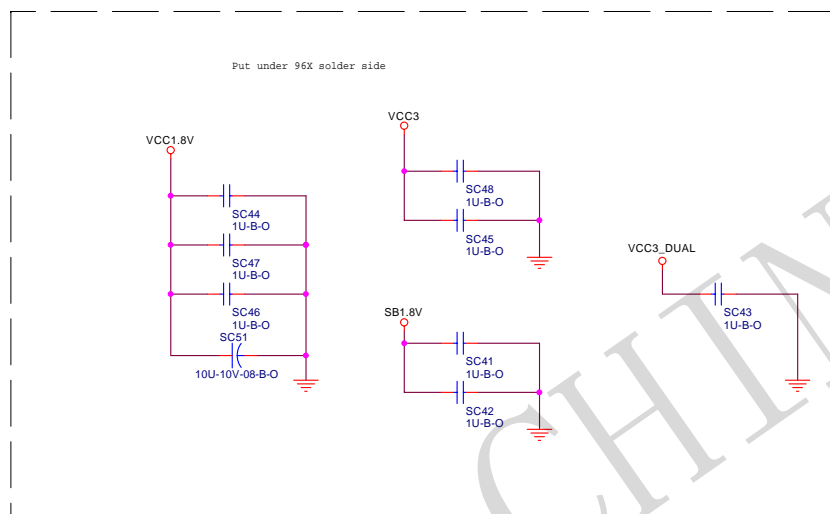


USB

964-3

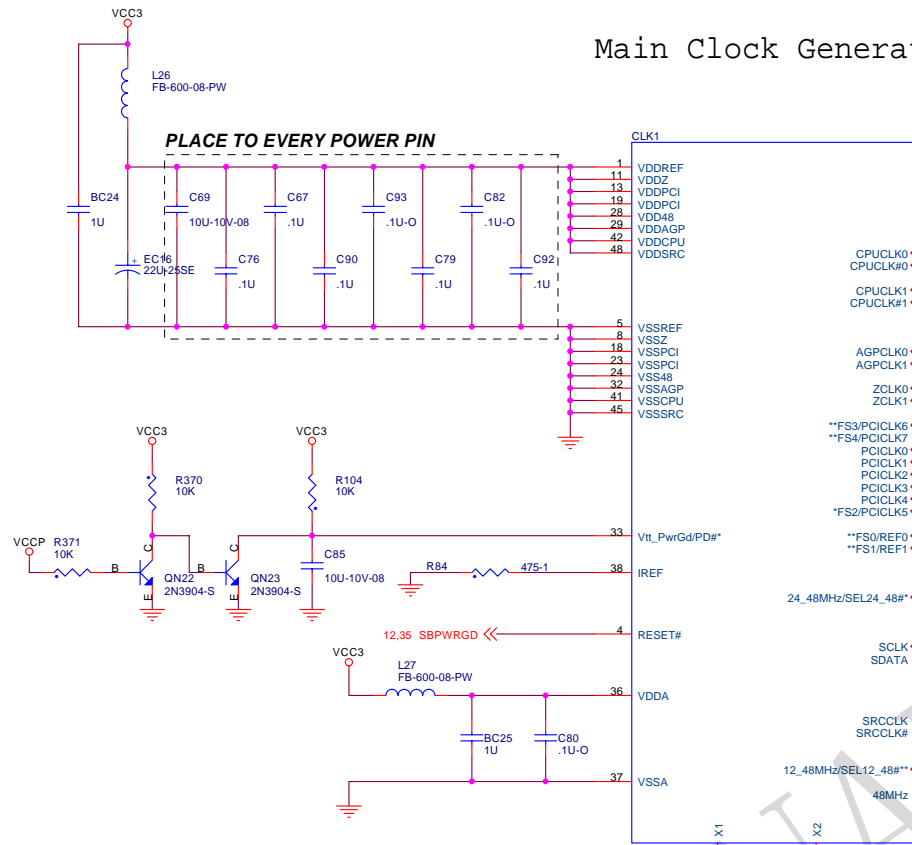
3.3 0mA



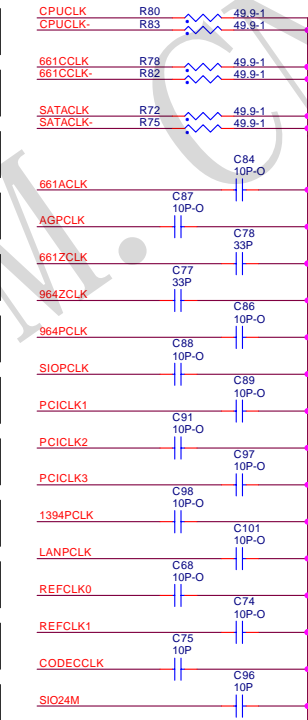


Power

Main Clock Generator



By-Pass Capacitors Place near to the Clock Outputs



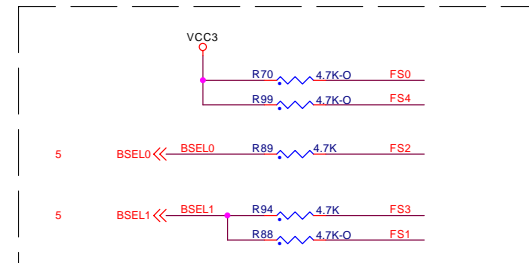
Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
0	0	0	0	0	100.00	100.00	133.33	66.67	33.33
0	0	0	0	1	100.99	100.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	0	1	0	0	133.33	100.00	133.33	66.66	33.33
0	0	1	0	1	134.65	100.99	134.65	67.32	33.66
0	0	1	1	0	137.33	103.00	137.33	68.66	34.33
0	0	1	1	1	133.33	100.00	133.33	66.67	33.33
0	1	0	0	0	200.00	100.00	133.33	66.67	33.33
0	1	0	0	1	201.98	100.99	134.65	67.33	33.66
0	1	0	1	0	206.00	103.00	137.33	68.67	34.33
0	1	0	1	1	200.00	100.00	133.33	66.67	33.33
0	1	1	0	0	166.66	125.00	125.00	66.66	33.33
0	1	1	0	1	168.31	126.23	126.23	67.32	33.66
0	1	1	1	0	171.66	128.74	128.74	68.66	34.33
0	1	1	1	1	166.66	125.00	125.00	66.66	33.33

Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
1	0	0	0	0	105.00	105.00	140.00	70.00	35.00
1	0	0	0	1	107.00	107.00	142.67	71.33	35.67
1	0	0	1	0	109.00	109.00	145.33	72.67	36.33
1	0	0	1	1	110.00	110.00	146.67	73.33	36.67
1	0	1	0	0	140.00	105.00	140.00	70.00	35.00
1	0	1	0	1	142.66	107.00	142.67	71.33	35.67
1	0	1	1	0	145.33	109.00	145.33	72.66	36.33
1	0	1	1	1	146.66	110.00	146.66	73.33	36.67
1	1	0	0	0	210.00	105.00	140.00	70.00	35.00
1	1	0	0	1	214.00	107.00	142.67	71.33	35.67
1	1	0	1	0	218.00	109.00	145.33	72.67	36.33
1	1	0	1	1	220.00	110.00	146.67	73.33	36.67
1	1	1	0	0	266.66	100.00	133.33	66.67	33.33
1	1	1	0	1	269.33	101.00	134.67	67.33	33.67
1	1	1	1	0	274.66	103.00	137.33	68.67	34.33
1	1	1	1	1	266.66	100.00	133.33	66.67	33.33

Frequency Selection



Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	BSEL1	BSEL0	Low	Low
CPU=100 (BSEL[1:0]=00)	0	0	0	0	0
CPU=133 (BSEL[1:0]=01)	0	0	1	0	0
CPU=200 (BSEL[1:0]=10)	0	1	0	0	0

Elitegroup Computer Systems

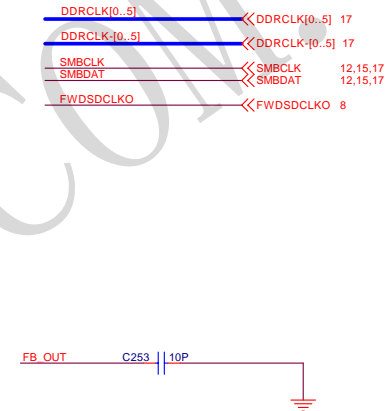
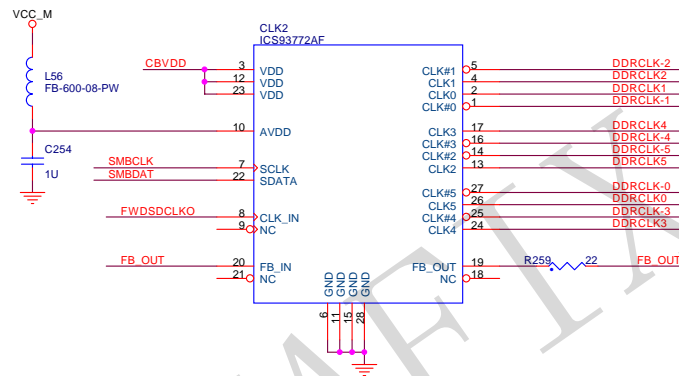
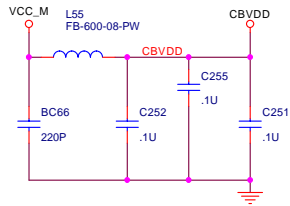
648(661)FX-M7

Size	Document Number	Rev
Custom	Main Clock	A
Date:	Wednesday, May 19, 2004	Sheet 15 of 37

Clock Buffer (DDR)

(5 OPTIONS)
 1:: (ICS) ICS93716
 2:: (Winbond)
 3:: (ICWorks)
 4:: (IMI)
 5:: (AMI)

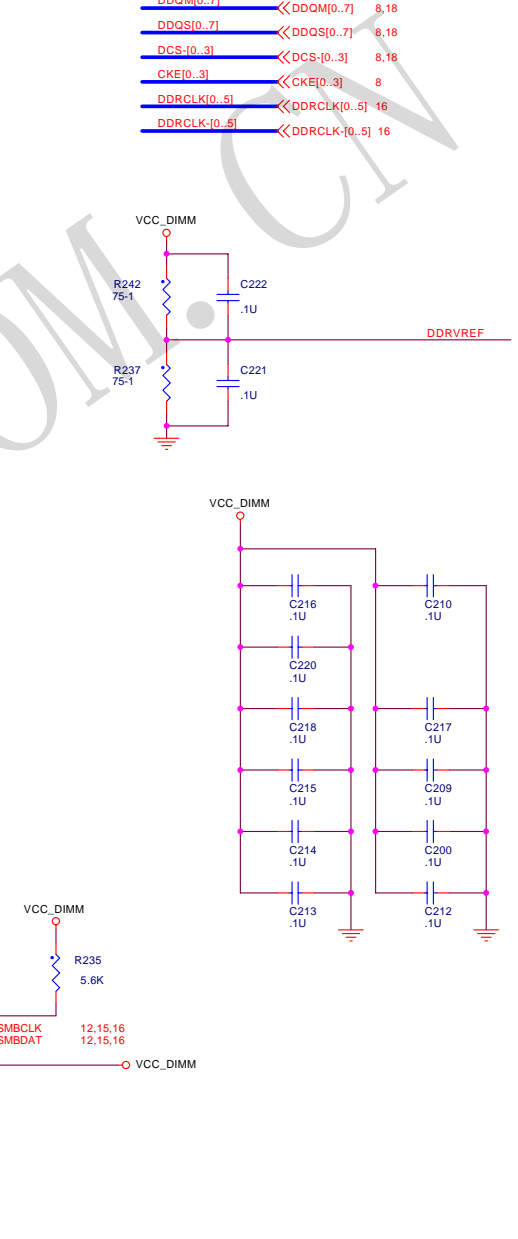
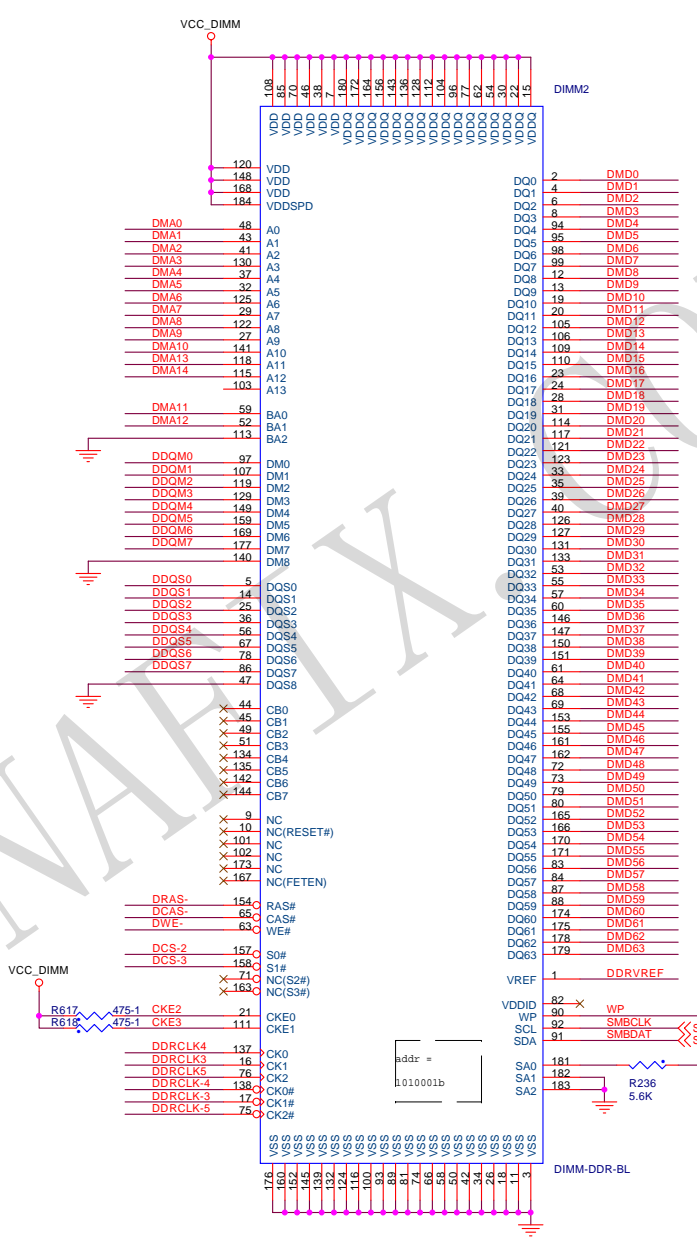
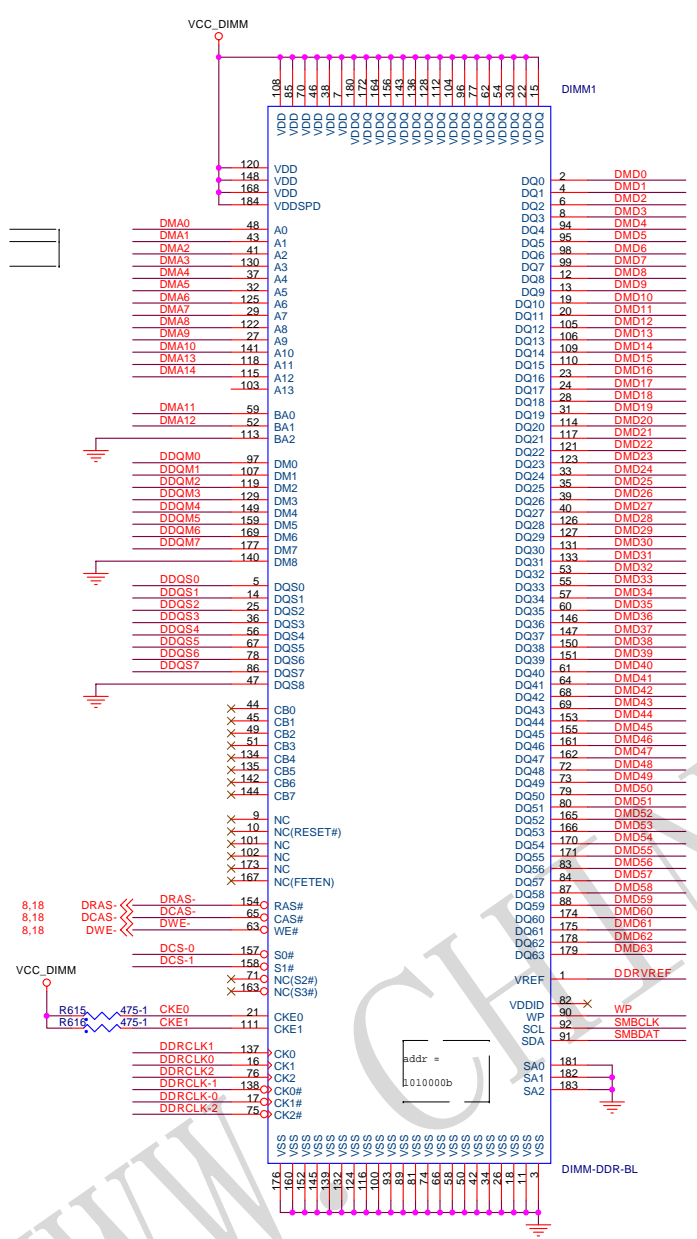
By-Pass Capacitors
 Place near to the Clock Buffer



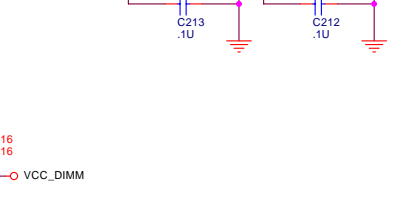
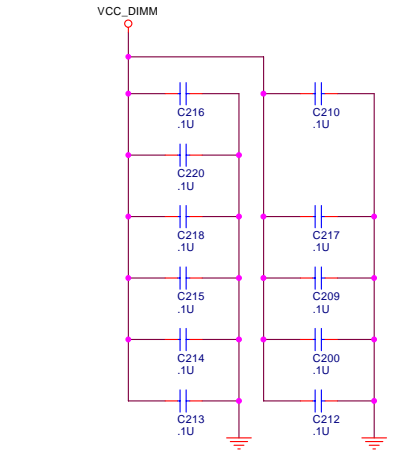
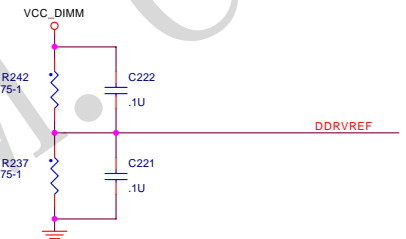
NOTE:
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:
VDDID VDD+VDDQ
OPEN VDDI=VDDQ
GND

MEMORY MUX TABLE:

SDR	DD
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	QSB0
CSB1	QSB1
CSB2	QSB2
CSB3	QSB3
CSB4	QSB4
CSB5	QSB5
CSB6	QSB6
CSB7	QSB7



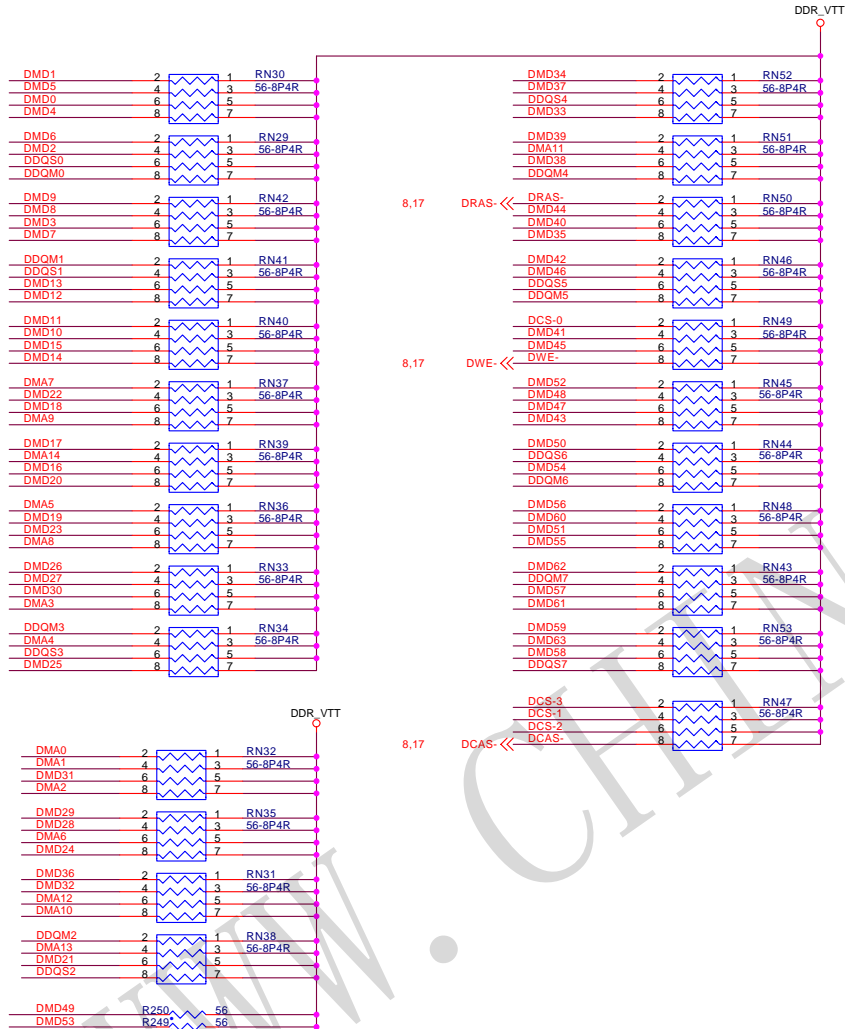
- DMD[0..63] << DMD[0..63] 8,18
- DMA[0..14] << DMA[0..14] 8,18
- DDQM[0..7] << DDQM[0..7] 8,18
- DDQS[0..7] << DDQS[0..7] 8,18
- DCS[0..3] << DCS[0..3] 8,18
- CKE[0..3] << CKE[0..3] 8
- DDRCLK[0..5] << DDRCLK[0..5] 16
- DDRCLK[0..5] << DDRCLK[0..5] 16



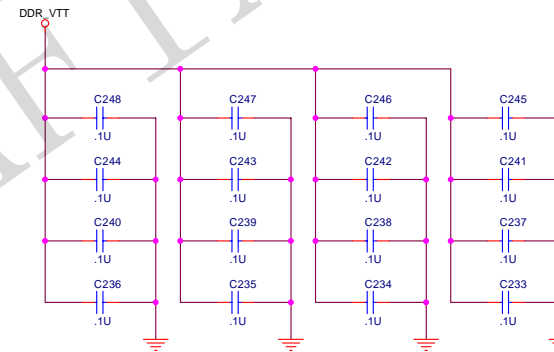
SSTL-2 Termination Resistors

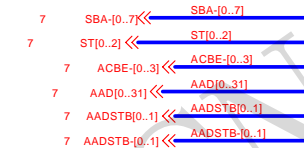
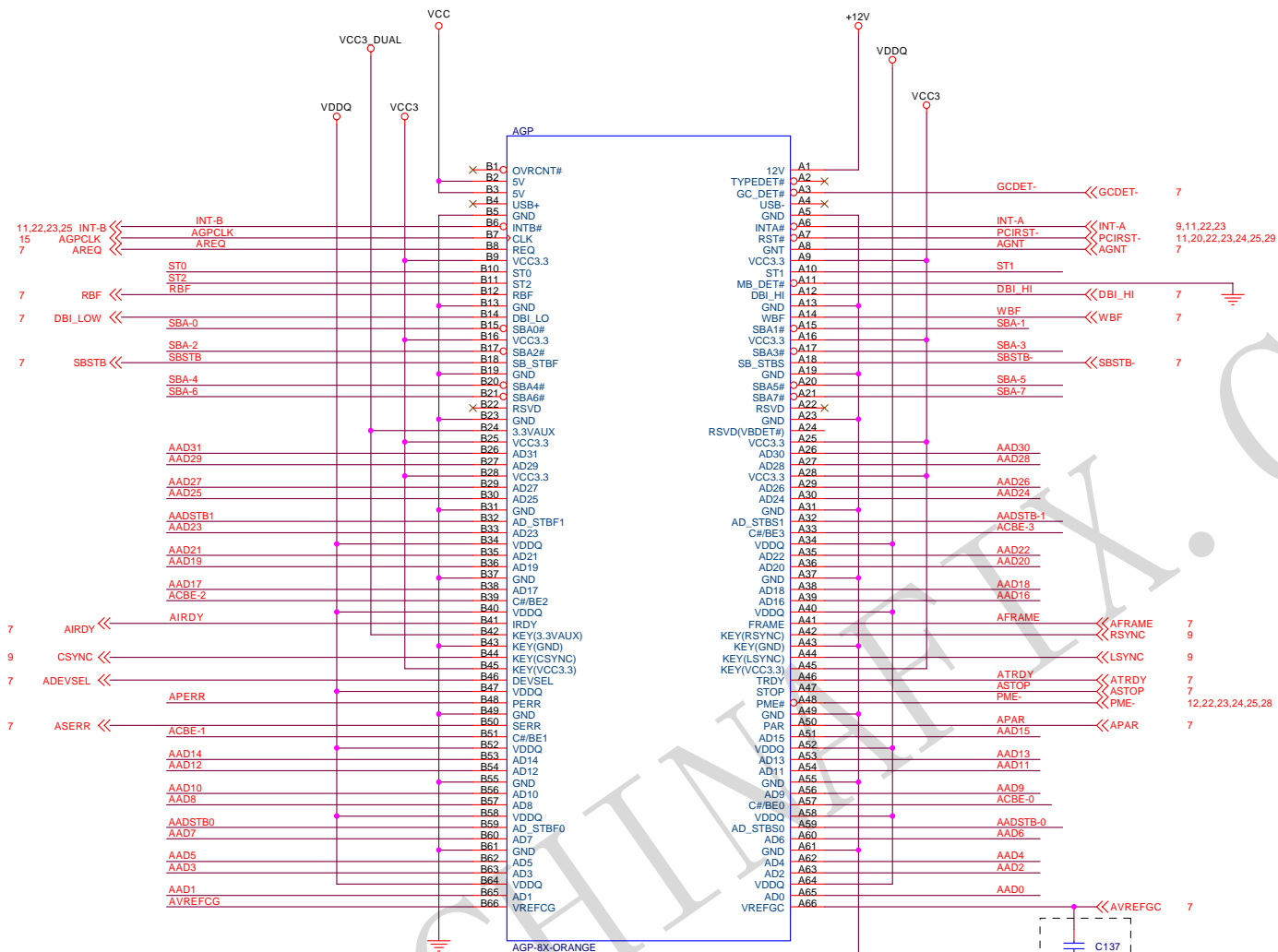
MD/DQM (/DQS)	LV-CMOS	Ra	0/10/-	DDR	Ra	10	Rtt	B3
MA/Control	LV-CMOS		10	SSTL-2				B3
CS	LV-CMOS		D	SSTL-2				B3
CKE	DD 3.3V			DD 2.5V				47

DMD[0..63]	<<DMD[0..63]	8,17
DMA[0..14]	<<DMA[0..14]	8,17
DDQM[0..7]	<<DDQM[0..7]	8,17
DDQS[0..7]	<<DDQS[0..7]	8,17
DCS-[0..3]	<<DCS-[0..3]	8,17

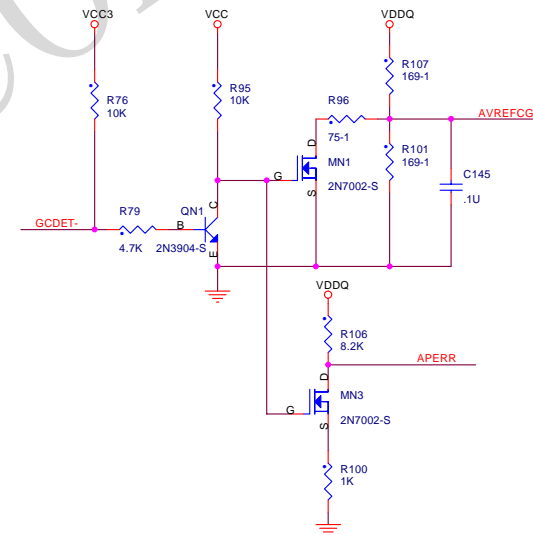


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs



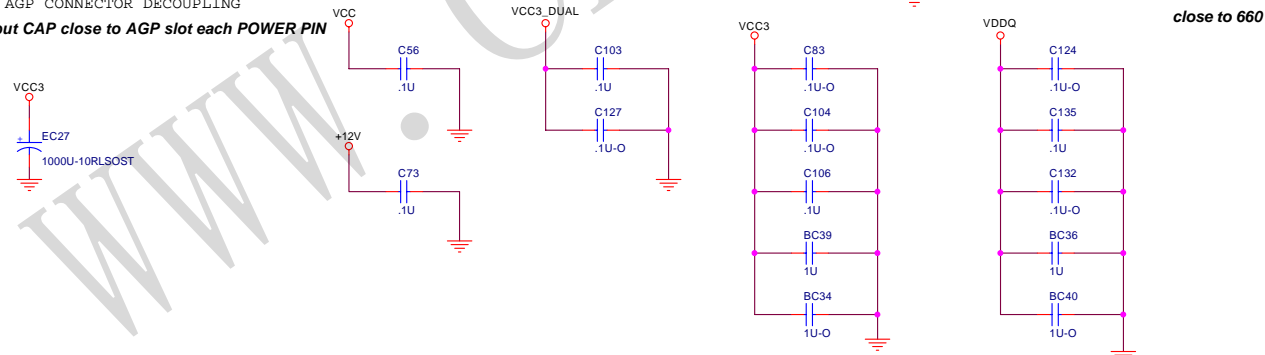


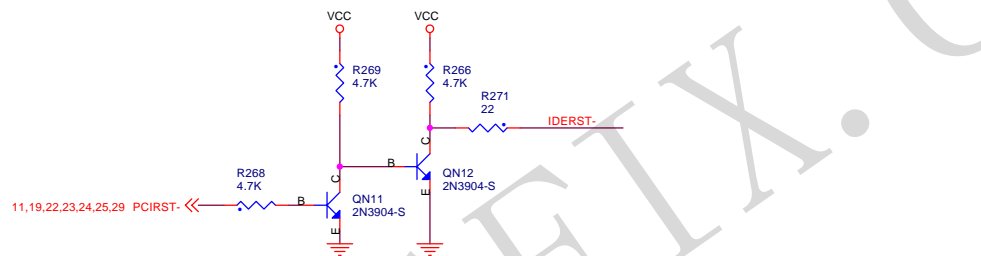
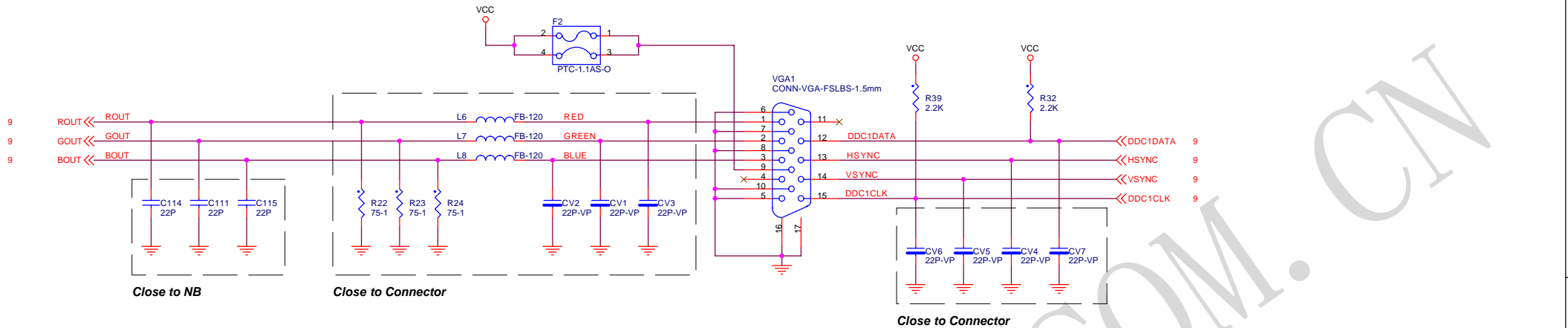
GCDET-	Low	Hi
Graphic Card	AGP 3.0	AGP 2.0
AVREFCG	0.35	0.75
APERR	0	1.5



AGP CONNECTOR DECOUPLING

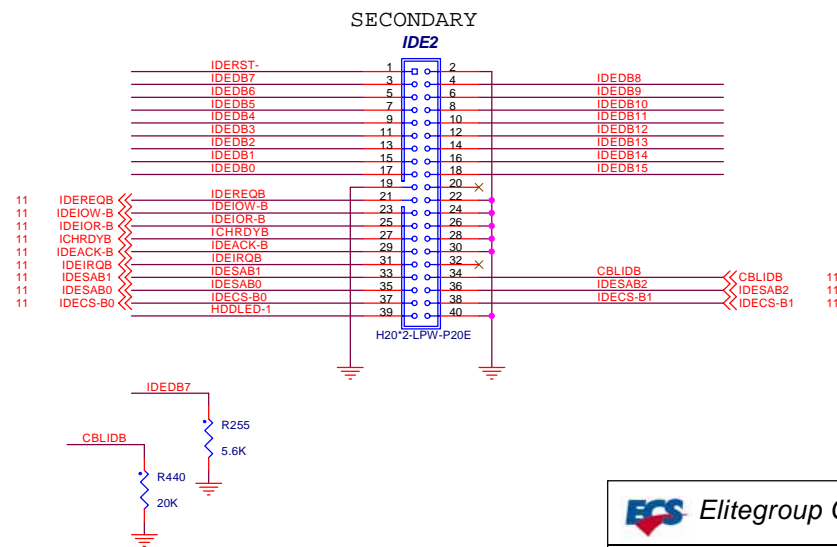
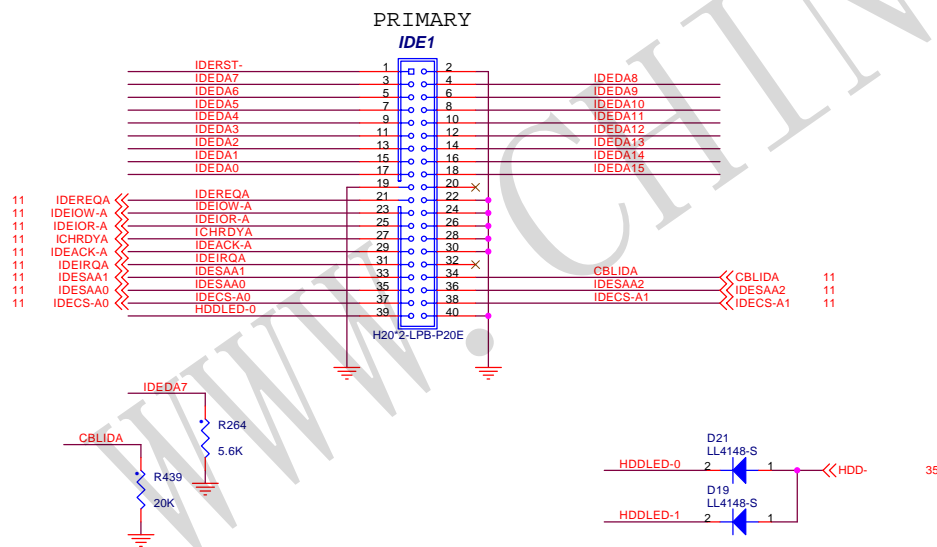
put CAP close to AGP slot each POWER PIN

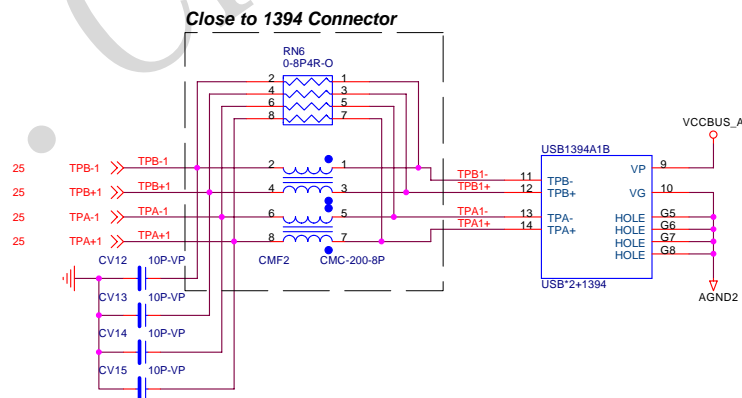
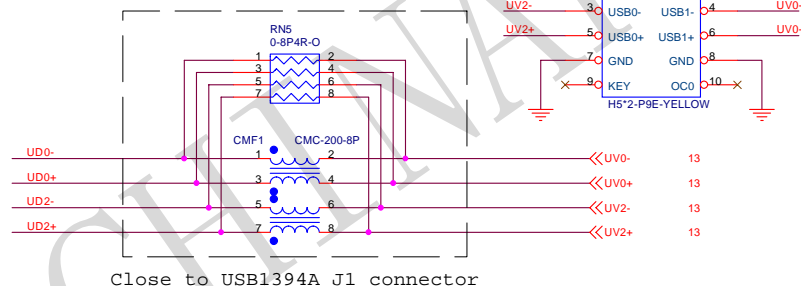
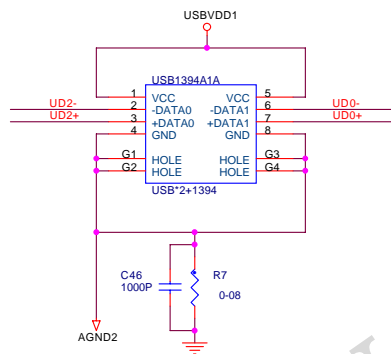
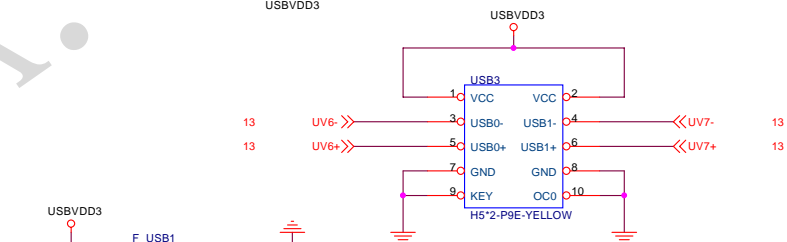
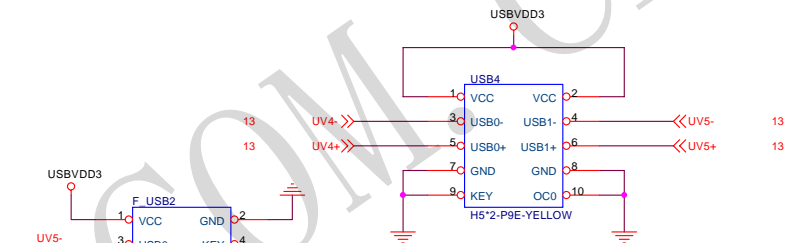
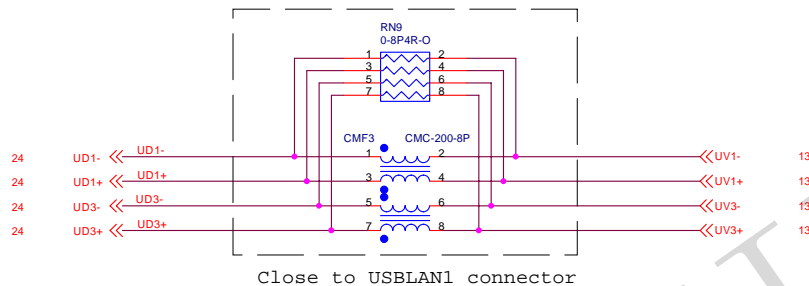
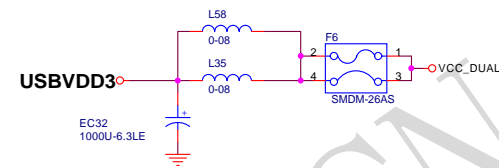
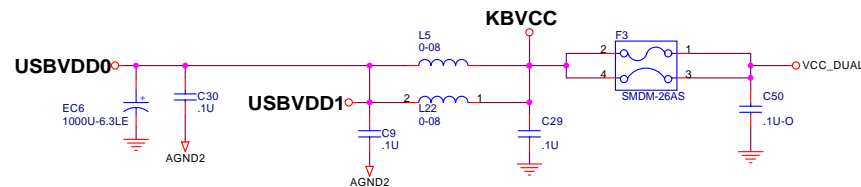
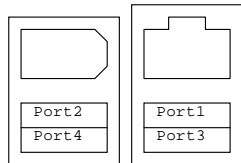




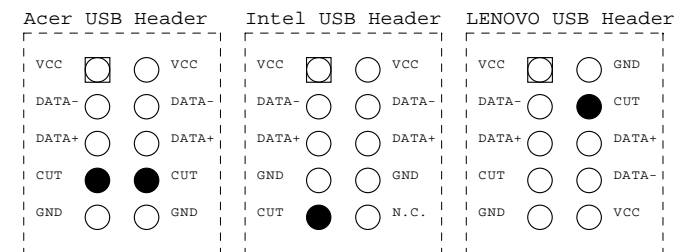
11 IDEDA[0..15] << IDEDA[0..15]

11 IDEDB[0..15] << IDEDB[0..15]

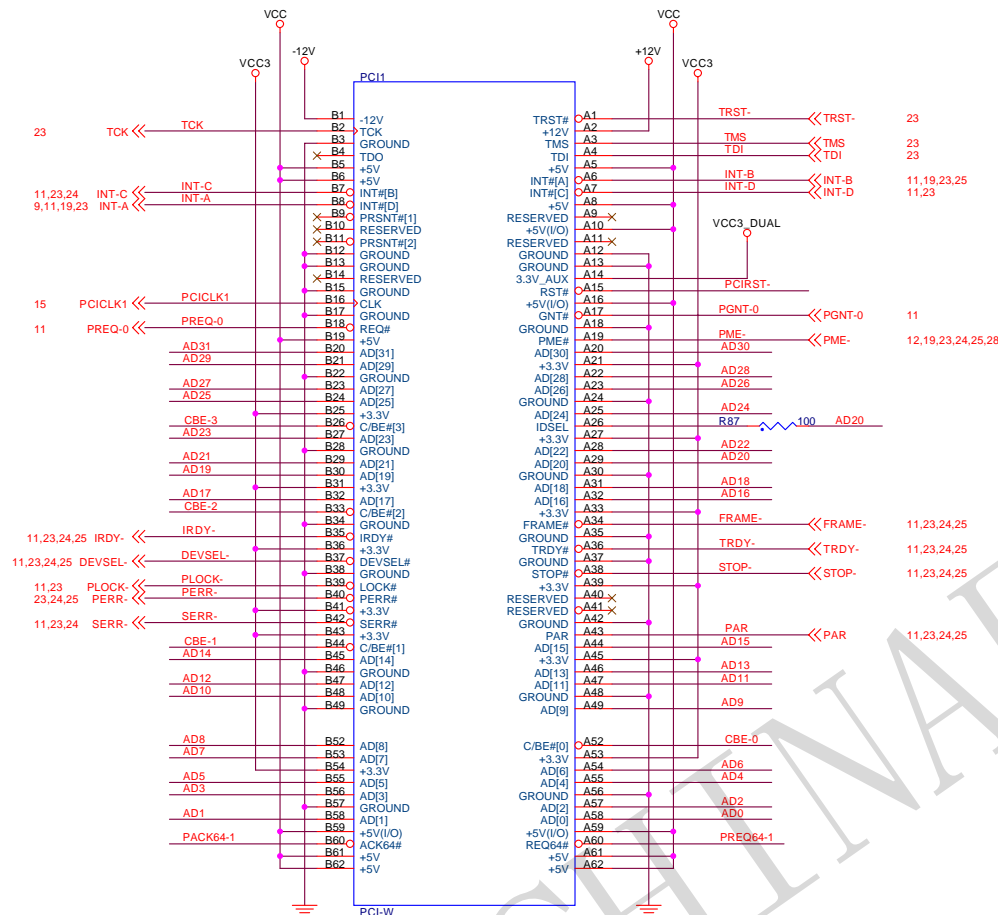




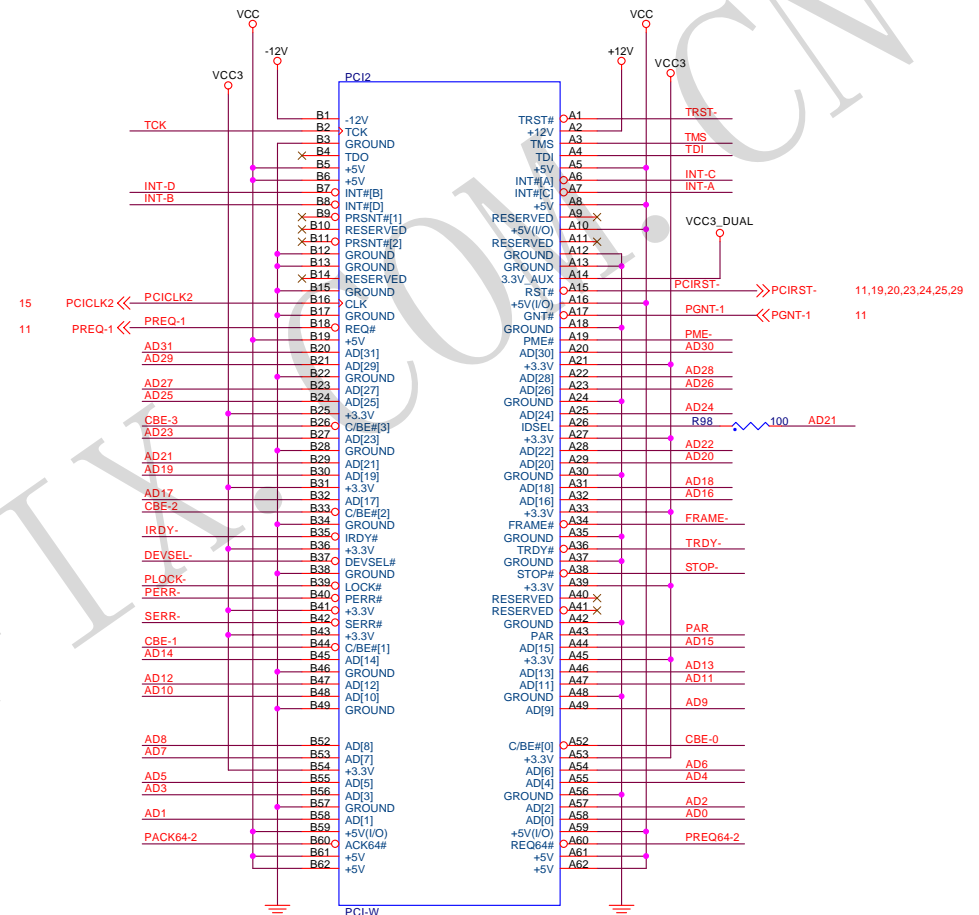
	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



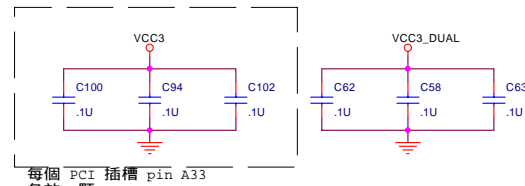
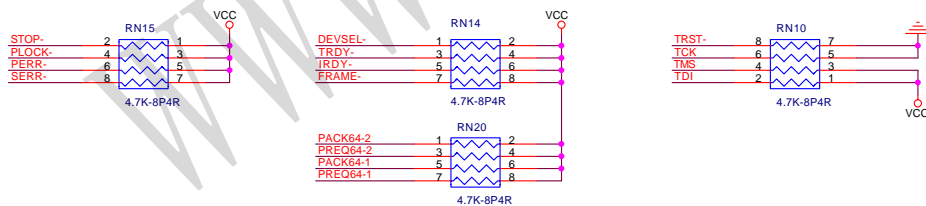
PCI Slot 1 & 2



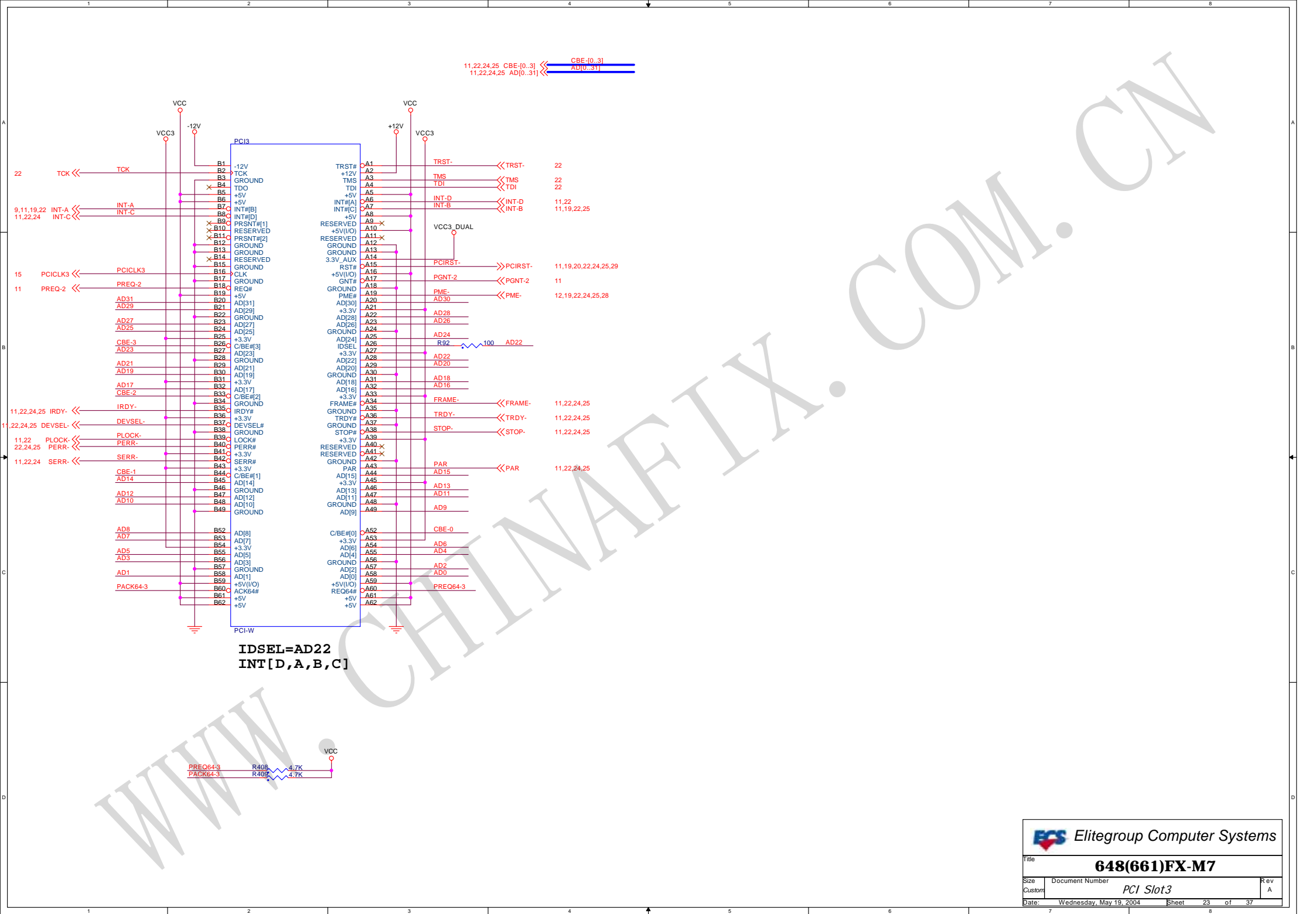
IDSSEL=AD20
INT[B,C,D,A]

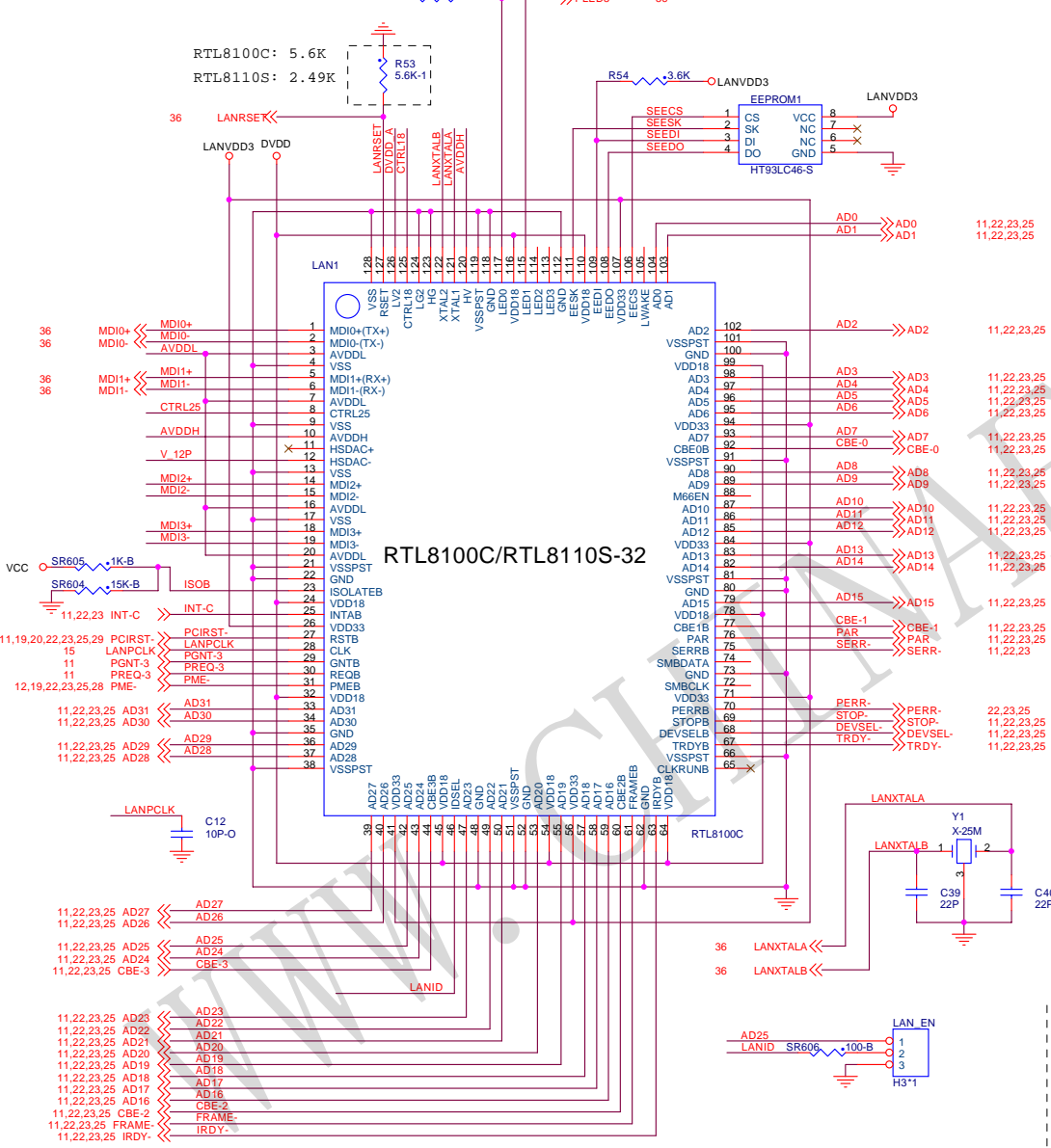
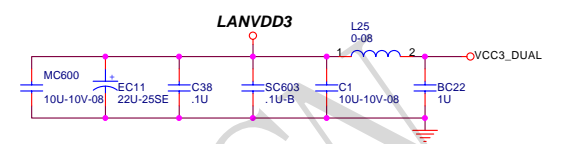
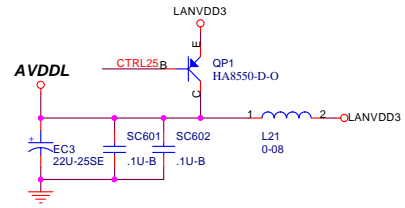
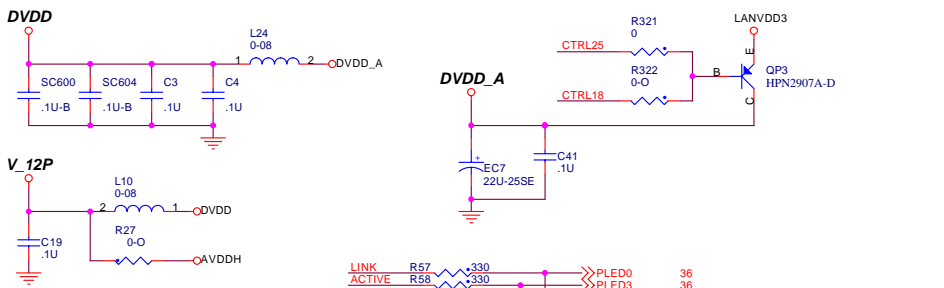


IDSSEL=AD21
INT[C,D,A,B]

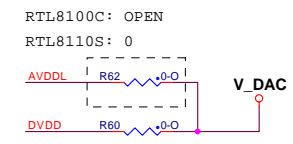


每個 PCI 插槽 pin A33
各放一顆

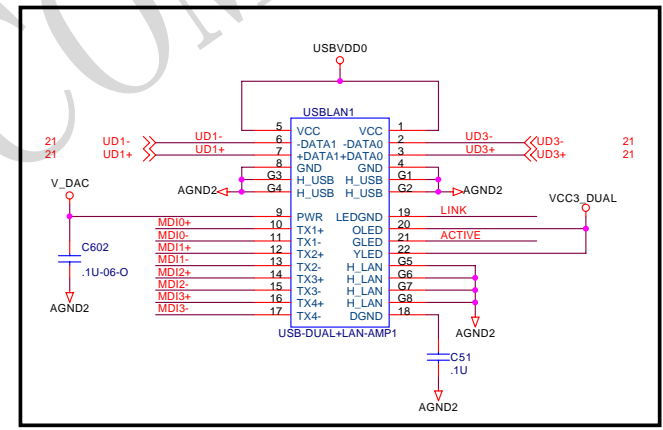




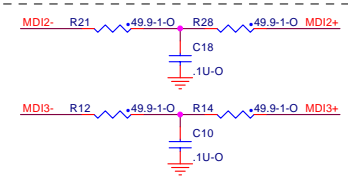
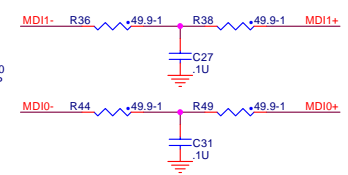
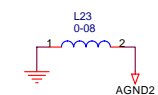
	8100C	8110S
VDD3	3.3V	3.3V
AVDDH	X	3.3V
AVDDL	3.3V	2.5V
DVDD_A	2.5V	1.8V
DVDD	2.5V	1.8V
V_12P	2.5V	X



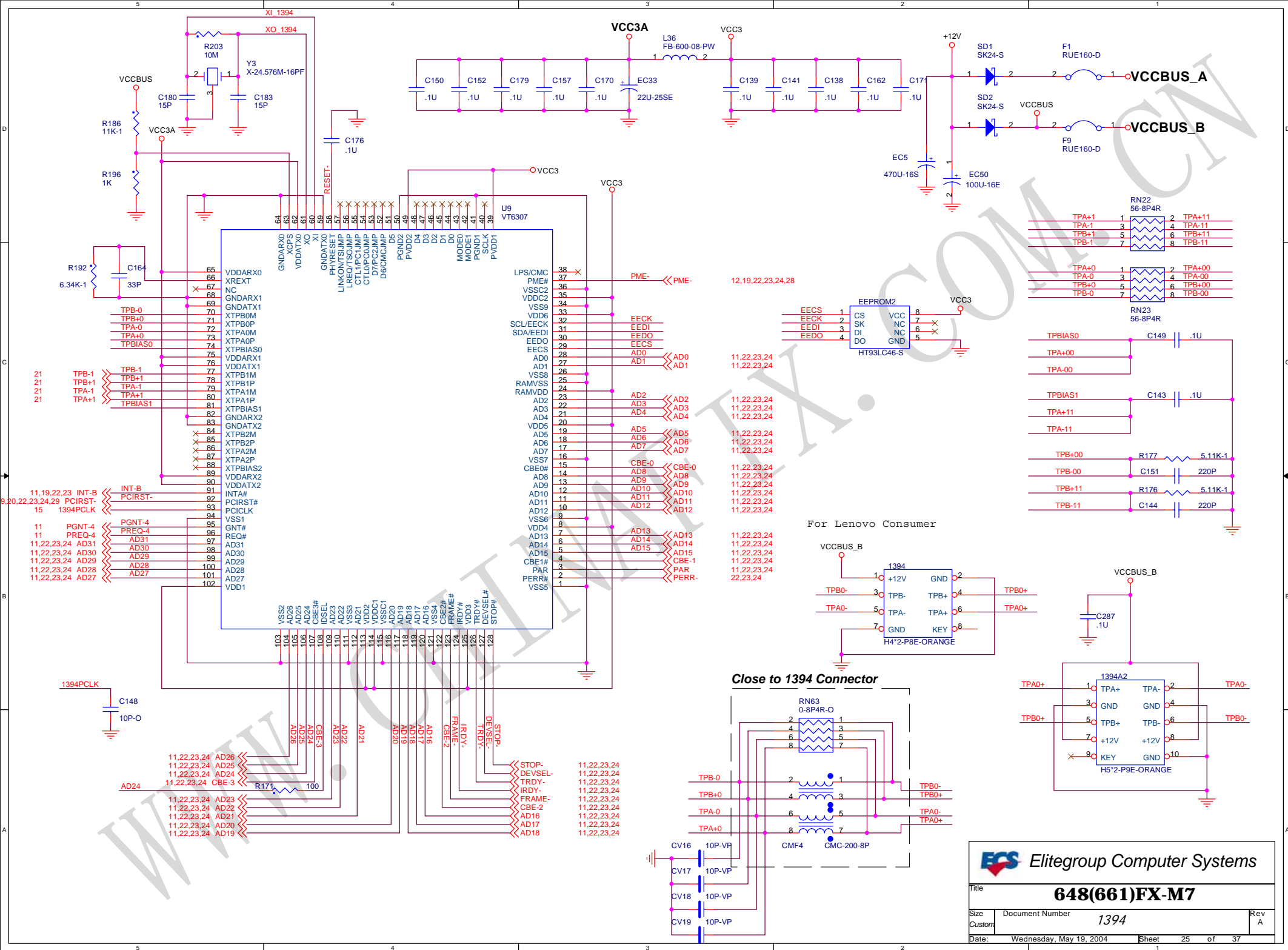
At RTL8100C application, remove R21, R28, R12, R14, C18, C10, C52, C53, C54, and change C51 value from .01uF to .1uF.

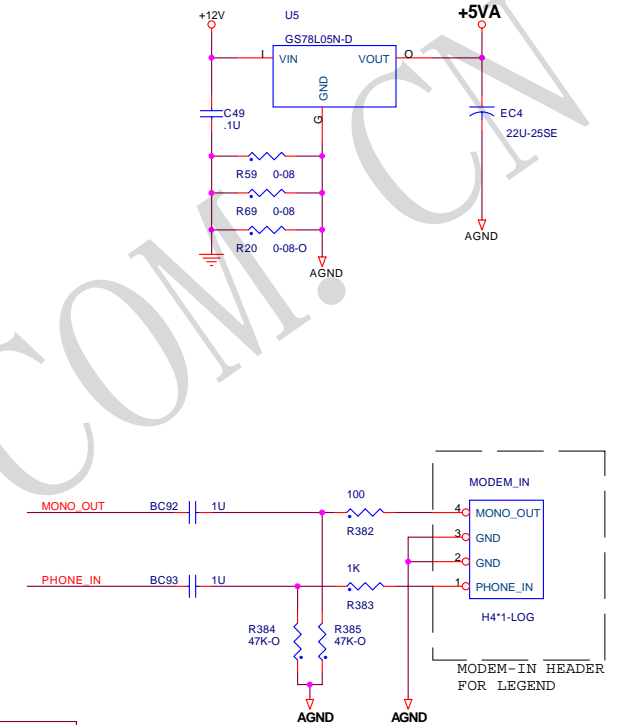
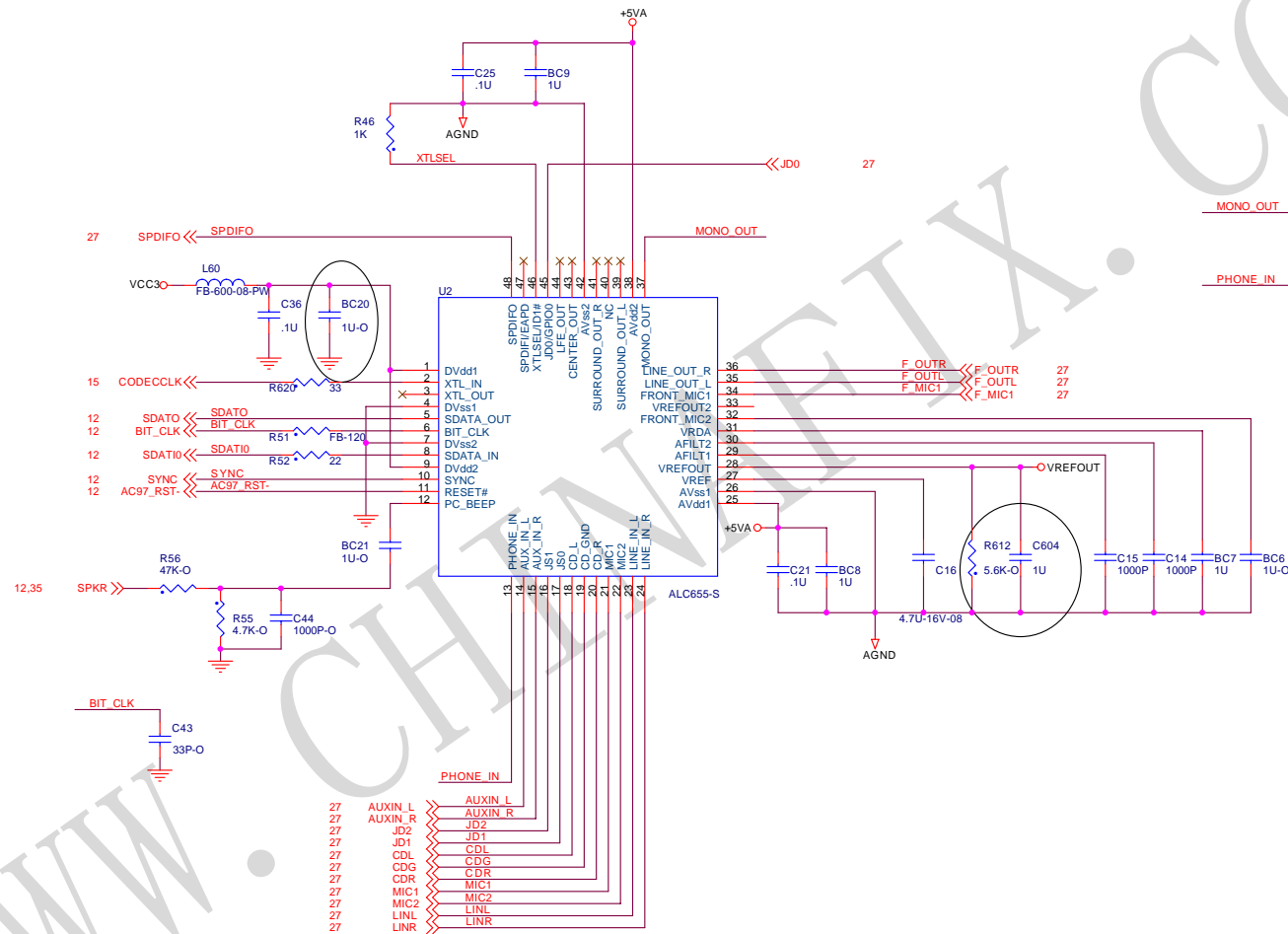


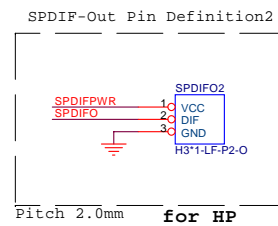
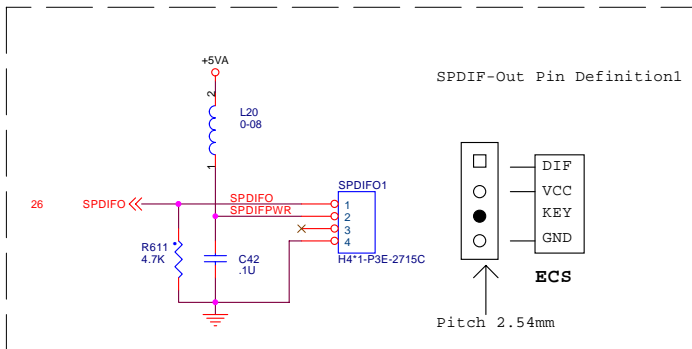
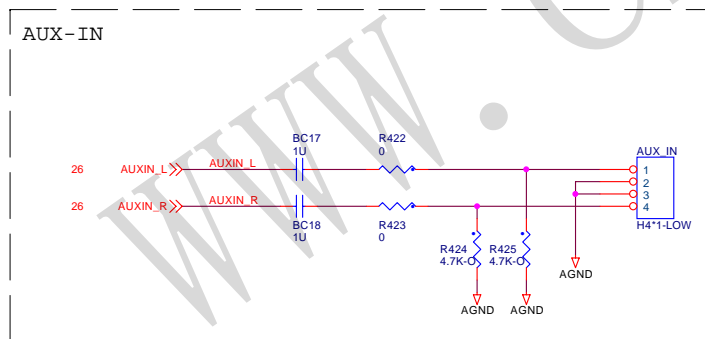
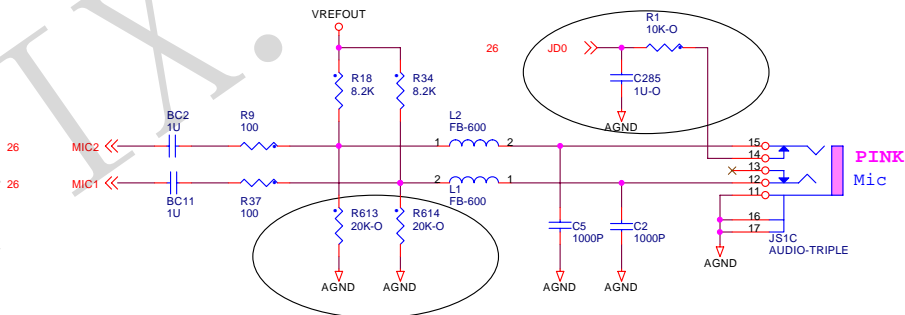
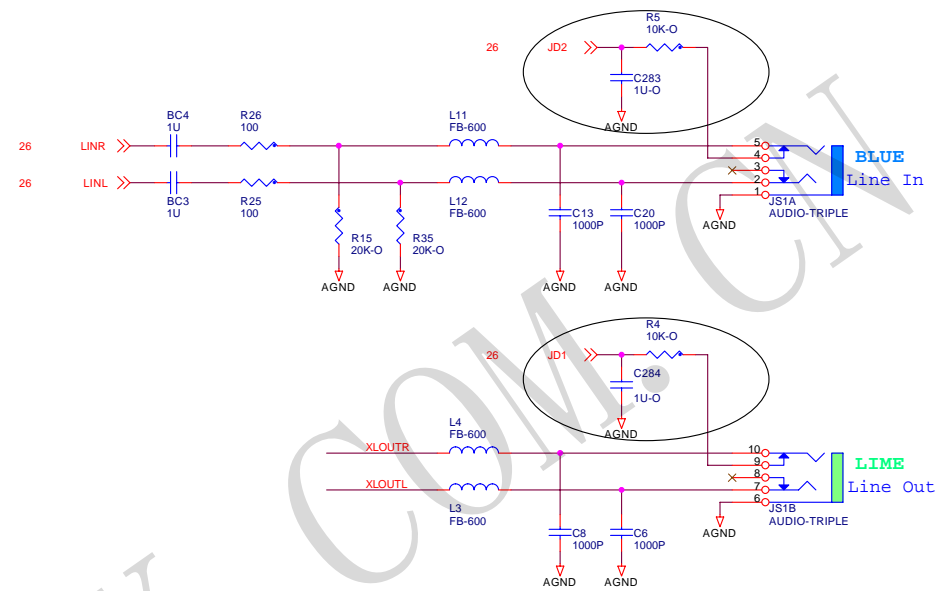
At RTL8100C application, use Pulse H1267.
At RTL8110S-32 application use Pulse H5007.

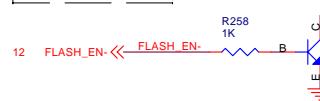
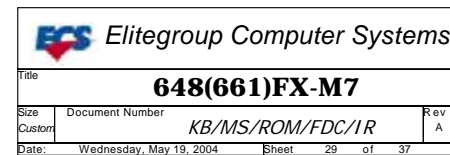


RTL8100C: OPEN
RTL8110S: Mounted

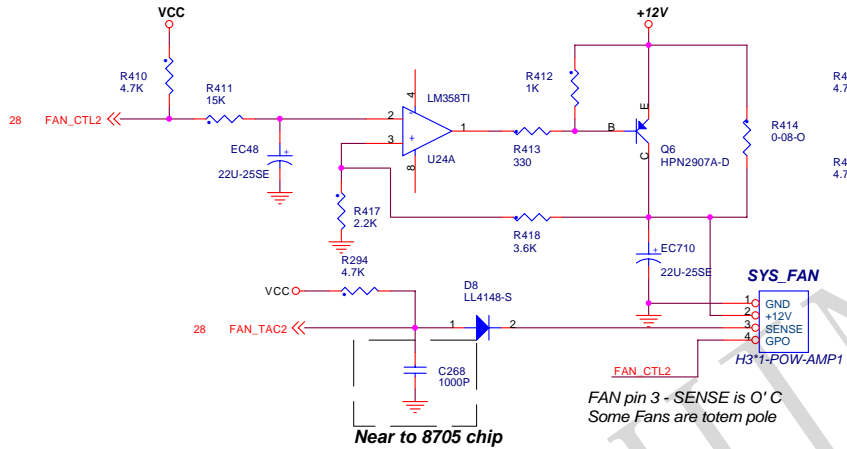
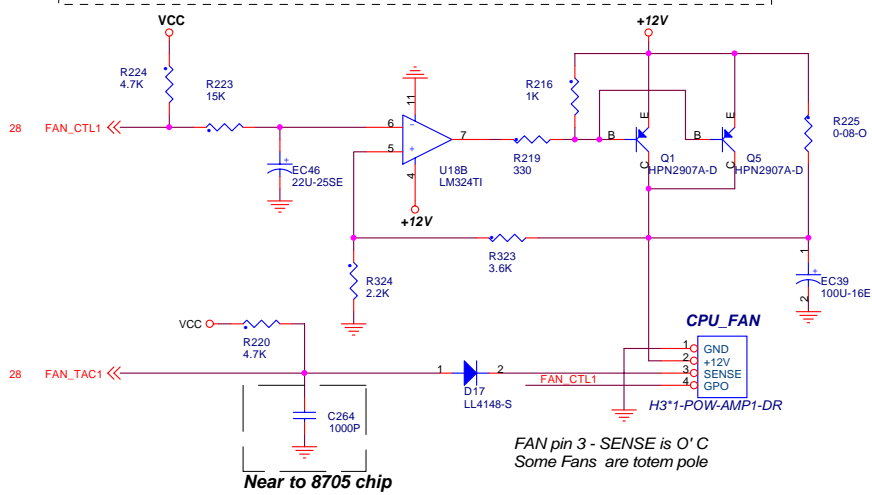




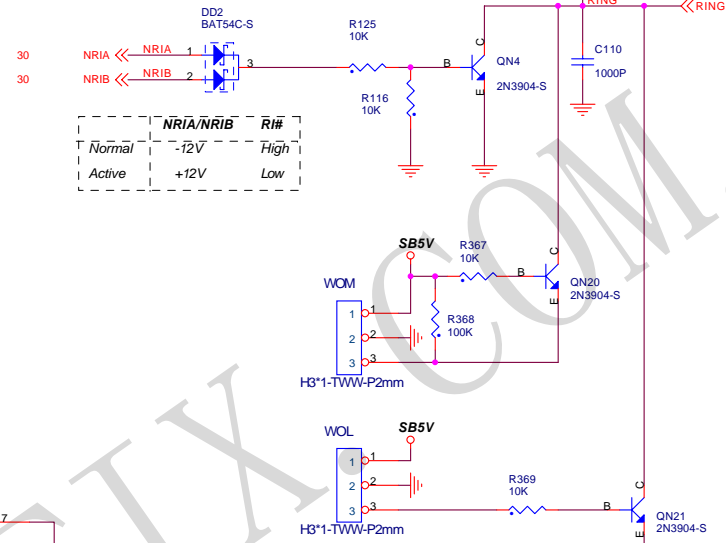
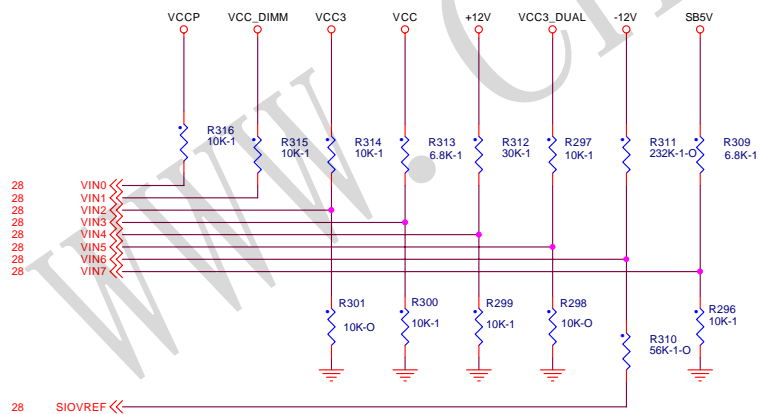


LPC INTERFACE
ROM

Layout :
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA.

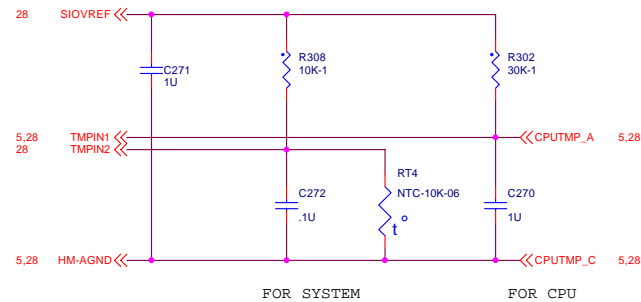


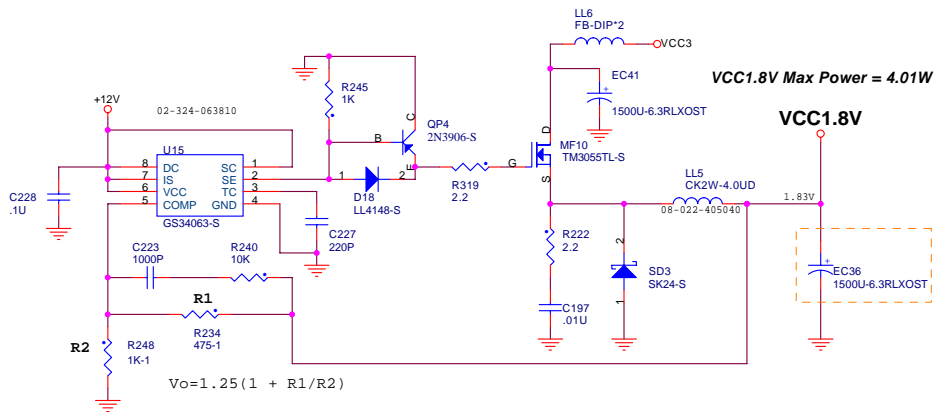
Voltage Monitor



Temperature Monitor

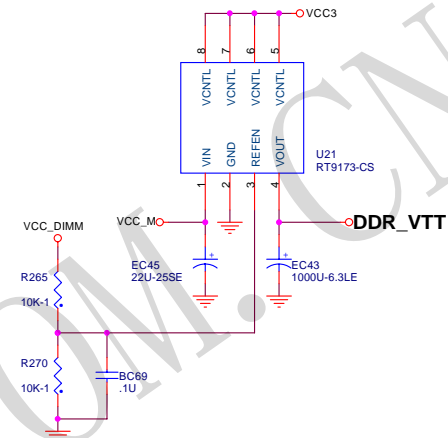
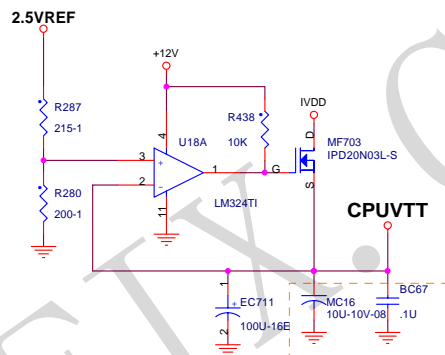
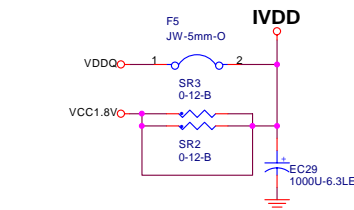
Choosing method of measuring temperature by either thermistor or diode



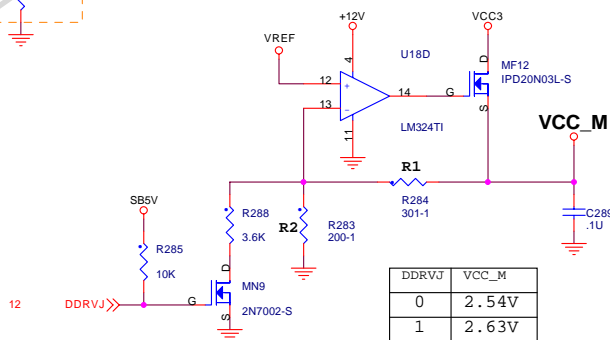
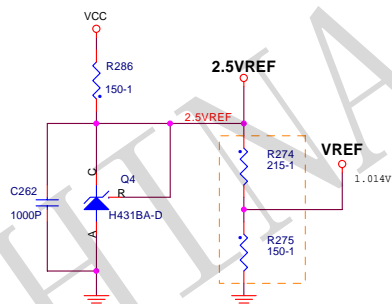
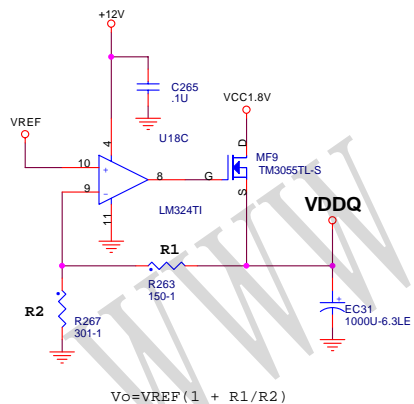


	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator

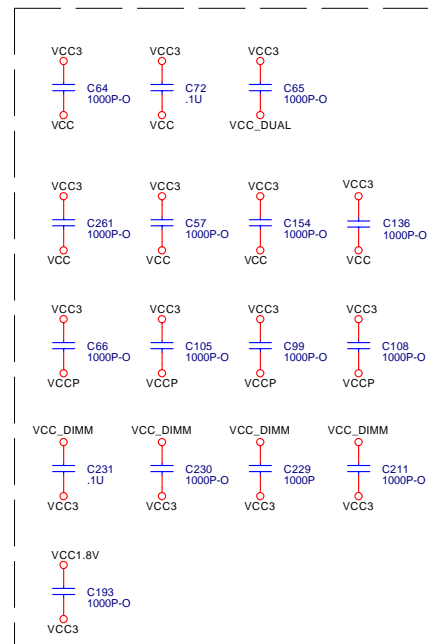
	AUX_IVDD	SB1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator



VCC1.5V Max Power = 0.3*(0.289+2.35)=0.7917W



DDR_VJ	VCC_M
0	2.54V
1	2.63V



平均分佈在POWER PLAN 和 PLAN 之間

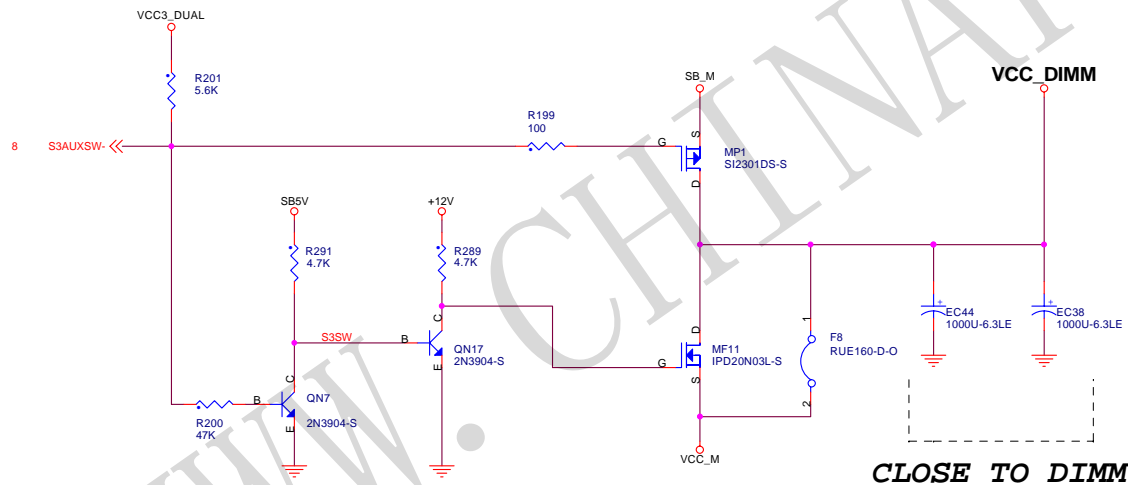
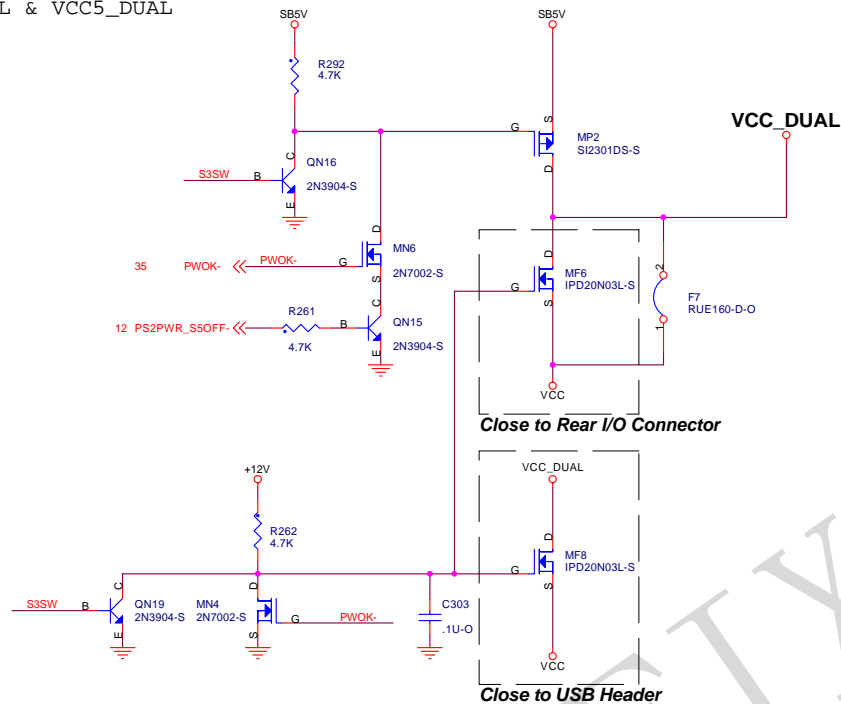
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

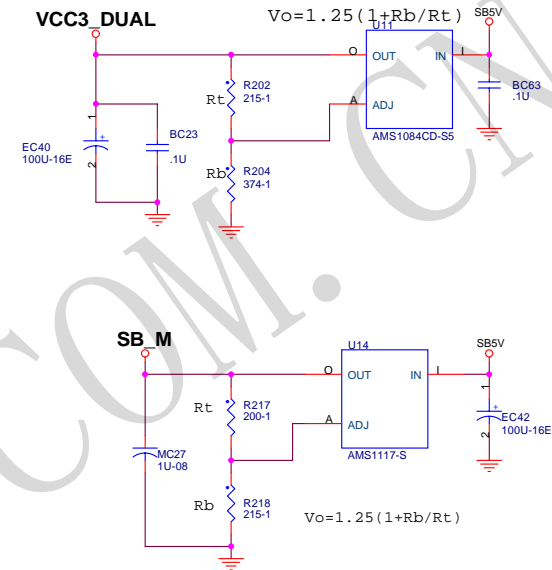
2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER. (ADDITIONAL
500mA PER USB PORT)

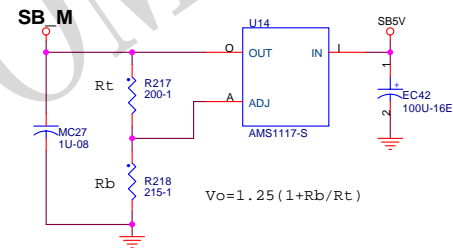
VCC3_DUAL & VCC5_DUAL



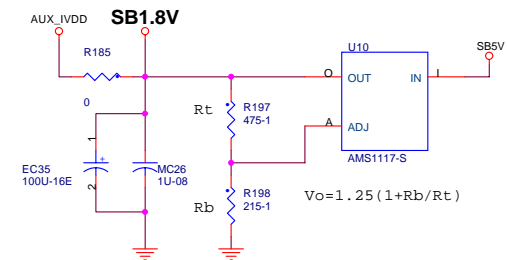
VCC3_DUAL



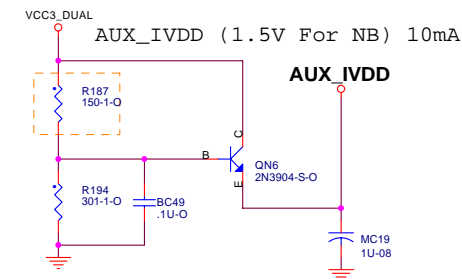
SB_M



SB1.8V (For SB) 450mA

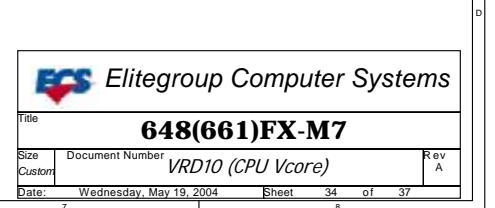
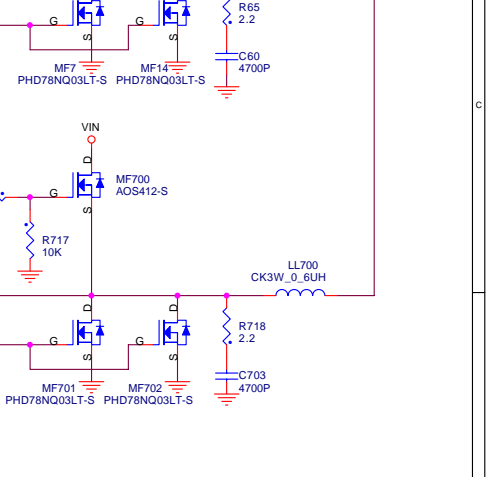
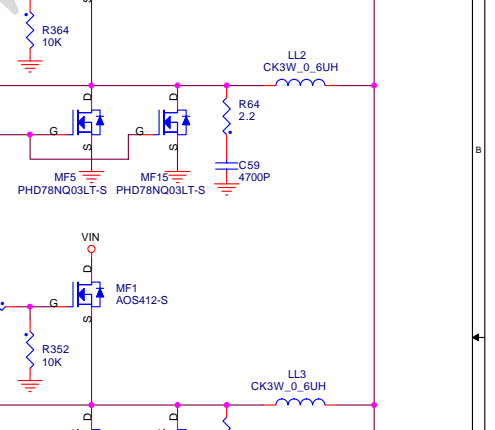
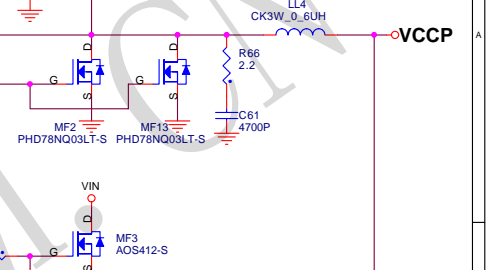
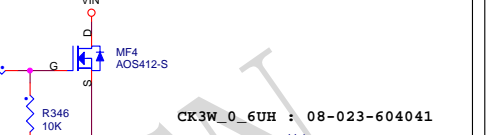
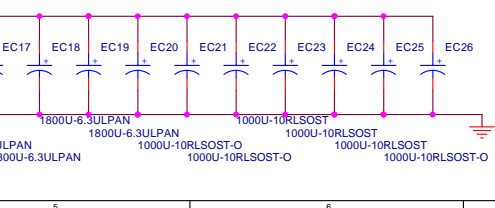
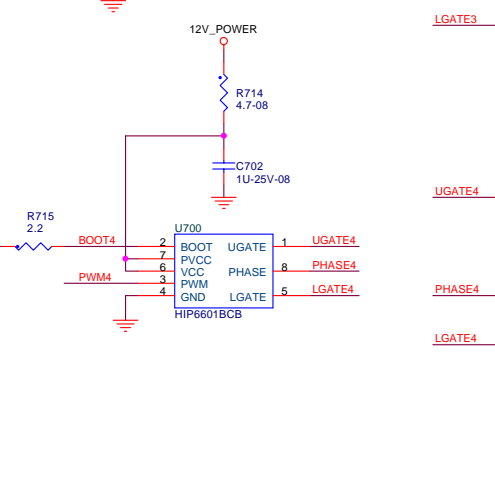
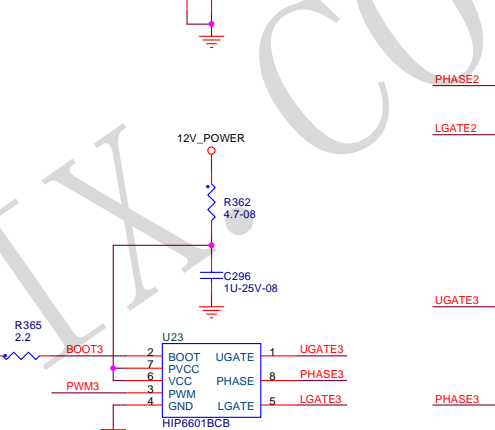
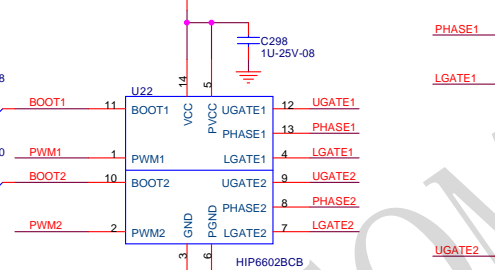
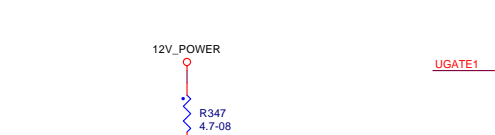
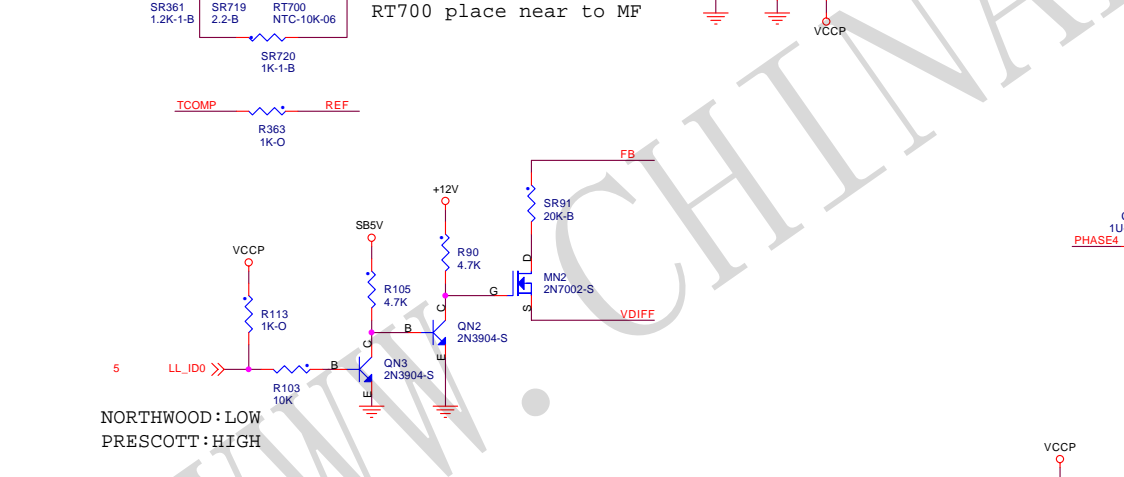
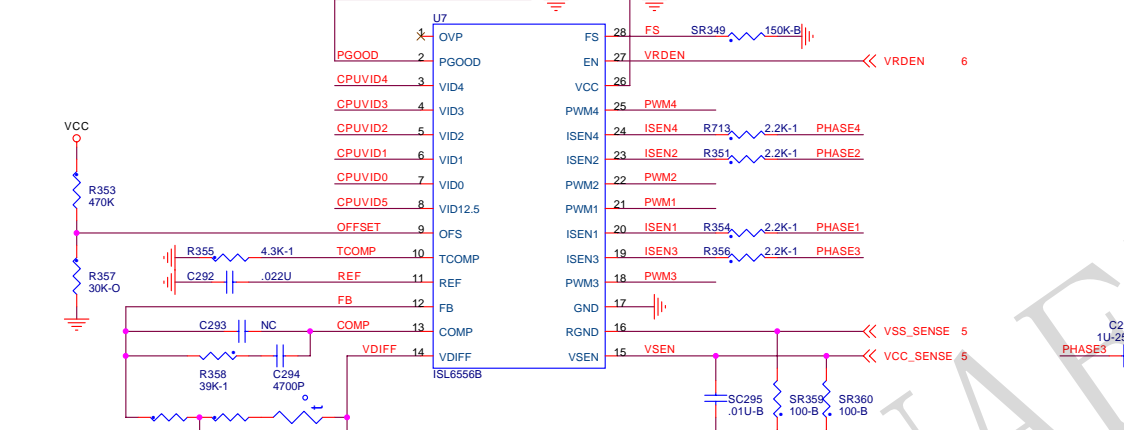
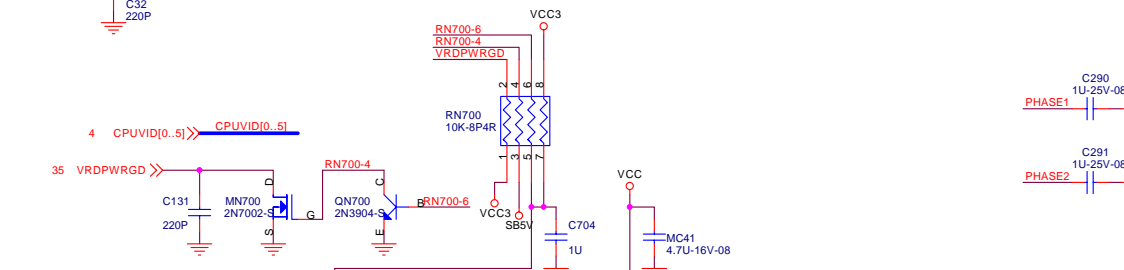
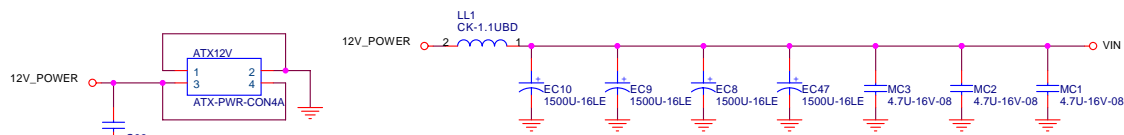


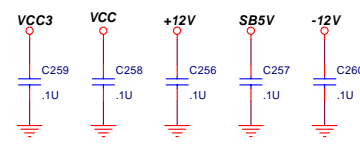
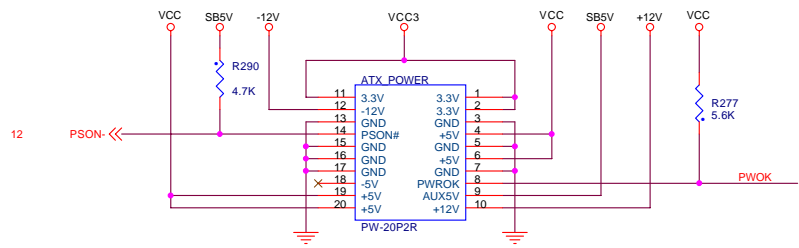
VCC3_DUAL



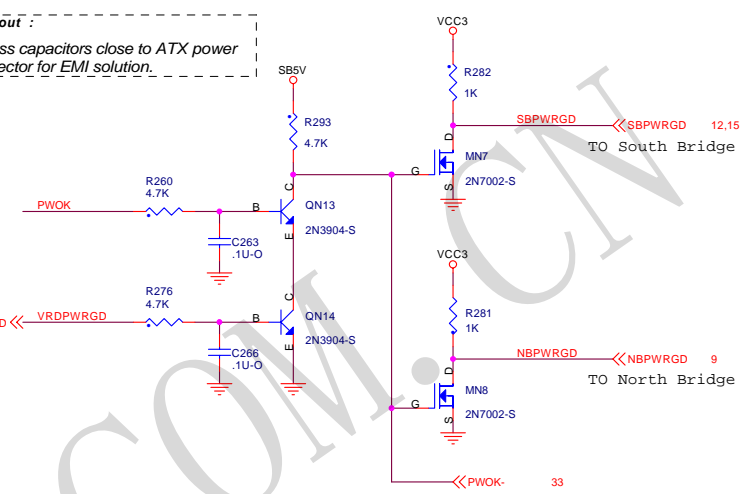
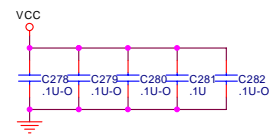
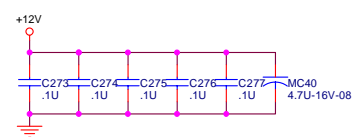
Elitegroup Computer Systems

Title			648(661)FX-M7
Size	Document Number	Dual 5V&3V, STR	
Custom		Rev	A
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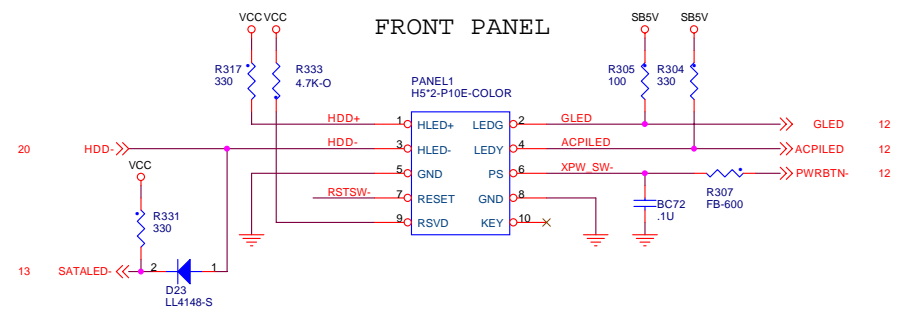


Layout :
Bypass capacitors close to ATX power connector for EMI solution.

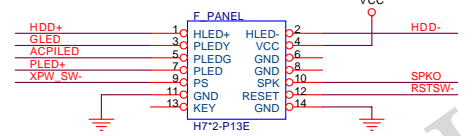
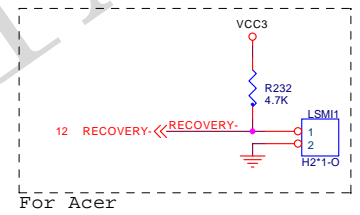
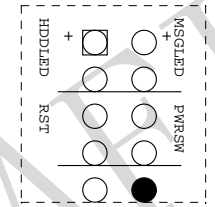


Hardware Reset Circuit

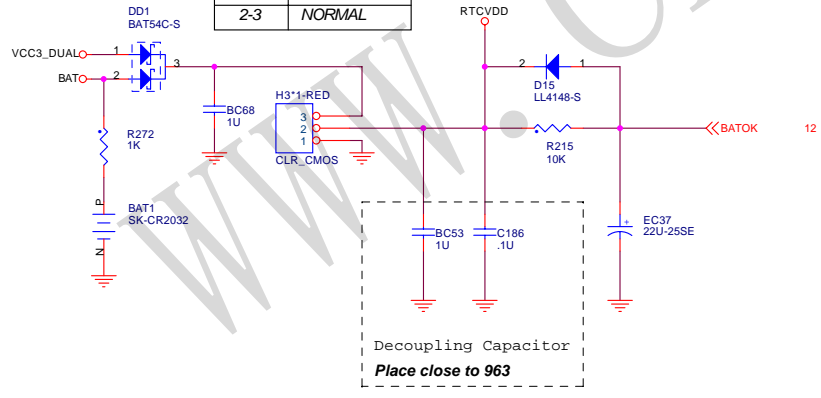
FRONT PANEL



Intel Front Panel

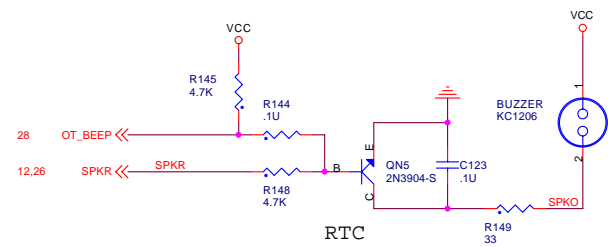


JP1	CLEAR CMOS
1-2	CLEAR
2-3	NORMAL

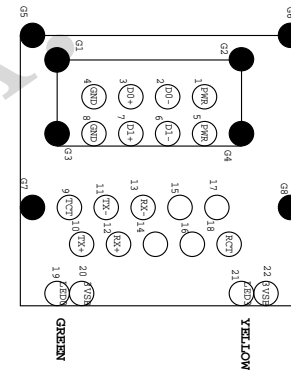


Decoupling Capacitor
Place close to 963

NOTE!
1.The RTCVDD is 3V
2.Decoupling capacitor must be close to 635 RTCVDD pin.
3.RTC circuit must strictly follow SiS's recommended design
SiS is not responsible for RTC problems from foreign designs.



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1. BOM Attention

(1) South Bridge

Option Components	SIS964	SIS964L
U13	964	964L
R241	374	X
R71, R74	33	X
R72, R75	49.9	X
R331	330	X
D23	1N4148	X
SATA1	O	X
SATA2	O	X

(2) LAN

Option Components	10/100 Mbps	1Gbps
LAN1	RTL8100C	RTL8110S
R53	5.6K	2.49K
R12, R14, R21, R28	X	49.9
C10, C18	X	0.1u
C51	0.1u	0.01u
C52, C53, C54	X	0.01u
RN62	75-8P4R	X
R62	X	0 ohm
T1	LF-H59X	HQ-H40B
L14	X	0 ohm
C23	X	0.1u
L21	0 ohm	X
QP1	X	HA8550
R321	0 ohm	X
R322	X	0 ohm
L10	0 ohm	X

(3) On-Board VGA

Option Components	Support	No Support
U8	661FX	648FX
L30, L31, L32	FB-120	X
C112, C116, C117, BC35	1U	X
C118, C119	.1U	X
MC36, MC37	10U	X
R136	130	X
R134, R143	33	X
R128, R135	100	X
VGA1	O	X
L6, L7, L8	FB-80	X
C111, C114, C115	22P	X
R22, R23, R24	75	X
R32, R39	2.2K	X
CV1-7	22P	X
F2	O	X
R234	475	169
R248	1K	301
R197	475	374
R198	215	200

2. GPIO Function

GPIO	Status	0	1	Jumper
GPIO5	* RESERVED	RESERVED	RESERVED	JP4
GPIO6	* RESERVED	RESERVED	RESERVED	JP5
GPIO7	* LAN Selection	LANPHY	PCILAN	N/A
GPIO9	USB, PS/2 S4/S5 Wake Up	Disable	Enable	N/A
GPIO10	DDR Voltage	2.54V	2.63V	N/A
GPIO11	* WHQL	No Support	Support	JPT3
GPIO13	Flash Write Protect	Un-Protect	Protect	

(1) "*" means that the function is selective and ECS may make changes at any time, without notice in this page.

(2) Jumper Setting (Header 3*1):

1: (1-2)

0: (2-3)

(3) Please see Page.12 for more detail jumper function.

